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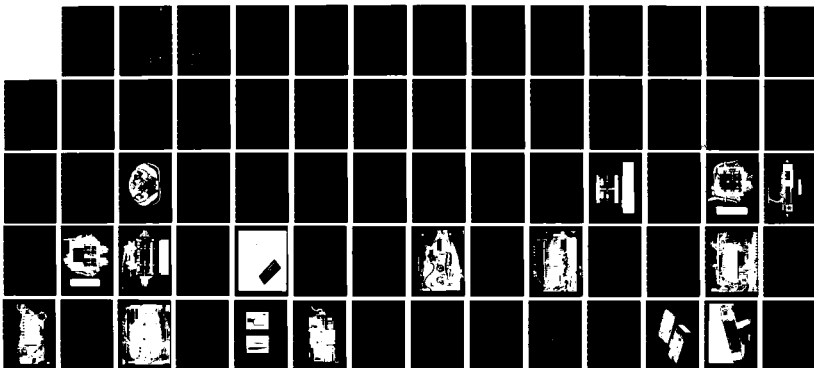
PORTABLE DIAGNOSTIC RADIOMETER(U) DAVID SARNOFF
RESEARCH CENTER PRINCETON NJ JUL 85 N00814-83-C-0524

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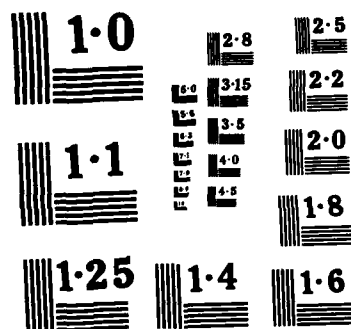
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NATIONAL BUREAU OF STANDARDS
MICROCOPY RESOLUTION TEST CHART

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AD-A157 685

PORTABLE DIAGNOSTIC RADIOMETER

FINAL REPORT - PHASE I

CONTRACT N00014-83-C-0524

PREPARED FOR

DEPARTMENT OF THE NAVY
NAVAL MEDICAL RESEARCH AND DEVELOPMENT COMMAND
NATIONAL NAVAL MEDICAL CENTER
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PREFACE

This Final Report for Phase I was prepared by RCA Laboratories, Princeton, New Jersey under Contract No. N00014-83-C-0524 for the Naval Medical Research and Development Command, Bethesda, Maryland. The work on Phase I was performed from October 1, 1983 through June 30, 1984 at the RCA Microwave Technology Center, Dr. Fred Sterzer, Director. The program was supervised by Markus Nowogrodzki, Head of the Microwave Subsystems and Special Projects Group. The Project Scientist was Robert W. Paglione, Member of the Technical Staff, with technical support provided by Francis J. Wozniak and Eugene C. McDermott.

The computer modeling and other software support was provided by Morris Ettenberg, Consultant.

I. INTRODUCTION

✓ There exists a need for a portable diagnostic instrument that can noninvasively monitor and display internal body temperatures. This instrument would be extremely important on U.S. Navy ships whose complement does not include the services of competent medical professionals. In this case it would be important to determine whether a particular medical emergency does or does not exist in a patient. This would determine whether the patient should or should not be evacuated to a suitable medical facility for treatment.

The instrument would determine, by radiometric means, whether particular organs exhibit an elevated temperature. For example, this may be an aid in the diagnosis of appendicitis or nephritis.

The instrument described in this report is a dual-frequency microwave radiometer. The radiometer measures the amount of noise power being radiated from a localized tissue volume on the patient. The amplitude of this noise power over a frequency spectrum determined by the microwave components is proportional to the average temperature of the volume in question. Making this measurement at two separate frequencies can give an indication of the temperature profile over a depth as great as 6 cm.



II. TECHNICAL DISCUSSION

A. PROGRAM OBJECTIVE

The objective of Phase I of this program was to develop a "proof of concept" breadboard of a dual-frequency radiometer. The instrument should include a microprocessor, a readout, a power supply, and all circuits necessary to prove the concept of a self-balancing, multifrequency radiometer suitable for use as a diagnostic instrument by the U.S. Navy.

To meet this objective, the following tasks would be addressed:

1. Computer modeling of a multifrequency radiometer to determine the optimum frequencies that, when used with the portable radiometer, would provide temperature information at three body depths where hot-spots indicative of inflammation could be detected.

2. Adapting the self-balancing radiometer circuits to provide the multifrequency mode of operation determined from 1.

3. Construction of a breadboard instrument model.

4. Evaluation and testing of the experimental instrument of 3.

B. COMPUTER MODELING

To be able to translate the multifrequency radiometric measurements of average temperature within a tissue volume into a three-point temperature profile, a computer model of the system and the resulting heat distributions as exhibited in particular radiometric measurements is required.

The computer program that has been developed calculates the

radiometric temperature at specified frequencies from a known temperature-versus-depth profile. The temperature profile is generated by assuming an arterial and ambient temperature and then calculating the heat transported due to the various heat conductivities and blood flows of the intervening tissue sections. The radiometric temperature is calculated in the following manner: The noise power, P_n , is calculated for a point on the temperature profile by multiplying the temperature, T_n , by Boltzmann's constant, k , and the receiver bandwidth, B . The amount of this power that reaches the surface is found by assuming an exponential decay with distance -- the exponential constant being the attenuation constant, α , of the intervening tissues. The radiometric temperature is then the sum of all of the surface noise powers generated by all of the points on the profile divided by kB . Mathematically this is written as

$$1) T_{RAD} = T_1 \{1 - \exp(-\alpha_1 x_1)\} + T_2 \{1 - \exp(-\alpha_2 x_2)\} \exp(-\alpha_1 x_1) + T_3 \{1 - \exp(-\alpha_3 x_3)\} \exp\{-(\alpha_1 x_1 + \alpha_2 x_2)\} + \dots + T_n \{1 - \exp(-\alpha_n x_n)\} \exp\{-\alpha_1 x_1 + \alpha_2 x_2 + \dots + \alpha_{n-1} x_{n-1}\}$$

where n = number of tissue sections

x = thickness of tissue section

and α = attenuation constant of tissue section.

The curve in Fig. 1 was generated by using the computer model and by assuming an arterial temperature of 37°C and an ambient temperature of 21°C . The tissue geometry used was taken from a body slice in the area of the appendix.¹ This slice,

shown in Fig. 2, contains skin, fat, muscle, intestine, the appendix (processus vermiformis), and bone. The front-to-back tissue thicknesses used in the model are: 1mm-skin, 8.5mm-fat, 6.55cm-intestine, 1cm-appendix, 3.3cm-muscle, 5.1cm-bone, 1.4cm-muscle, 1.05cm-fat, and 6.5mm-skin. Typical values were used for the tissue density, thermal conductivity, specific heat, and blood flow.² Also, a value was used for normal surface cooling.³ The curve in Fig. 1 is therefore a normal thermal profile in the appendix region. The radiometric temperature was calculated over the frequency range from 800 to 4000 MHz. The front surface reading is labeled TF(rad) in the figure, and only the 800 and 4000 MHz data are shown since the temperature function is linear between these two points.

In Fig. 3a, b, and c, the appendix has been given an elevated temperature of 2° over normal; and the position of the appendix is varied from 4 to 8 cm. It can be seen from this data and the data in Fig. 1 that the radiometer must have an accuracy of 0.2°C in order to detect a 2°C elevated temperature at a depth of 6 cm.

In Fig. 4 and 5, the radiometric temperatures at 800 and 4000 MHz are plotted as a function of the surface temperature and hot-spot depth. The line representing no hot spot (NHS) is also shown in both figures. Therefore, from the measurement of the surface temperature and the radiometric temperature at 800 and 4000 MHz, it is possible to determine the depth of a typical hot spot. The temperature profile can then be extracted from the computer model. For example, if the surface and radiometric

temperatures are 33.7°C , 36.7°C at 800 MHz, and 36.1°C at 4000 MHz; then the hot spot occurs at a depth of 4 cm. The temperature profile for this condition is as shown in Fig. 2b; and the three temperatures that would be displayed are 34.7°C at 0 cm depth, 37°C at 2 cm depth, and 38.7° at 4 cm depth.

C. 4 GHz SUBSYSTEM

The basic Dicke-type radiometer⁴ is shown schematically in Fig. 6. In this circuit, the target noise power entering through the antenna is compared to the noise power emanating from a temperature-controlled termination. The difference between the two signal levels is displayed on the DC meter--this reading is proportional to the temperature of the target. An improvement can be made in the accuracy of this system if the reference noise signal, in this case the oven-controlled termination, was always adjusted to give a zero reading on the DC meter; then the temperature of the reference noise source would be equal to the temperature of the target. This self-balancing scheme can be realized by replacing the over-controlled termination with a diode noise source. The mixer can also be replaced with a synchronous detector to improve the system sensitivity and reduce the system noise.

The single-throw-double-pole switch is usually realized with an electronically-switched, latching ferrite circulator; however, at these frequencies, the size, weight and current drawn by these components are limiting factors when considering a portable instrument. The switch can also be designed using switched low-noise amplifiers, as shown in Fig. 7. Each amplifier is pulsed

on and off asynchronously with the other, and the off-channel isolation is greater than 40 dB. The output of each amplifier is combined through a 3 dB hybrid coupler to produce a single switched output.

The amplifiers were designed around the NE13783-4 field-effect transistor--these transistors are optimized for low-noise performance at 4 GHz. The scattering parameters of these devices were measured with a computer-controlled automatic network analyzer. Input and output matching networks were designed that would produce an amplifier with a minimum gain of 13 dB from 3.7 to 4.2 GHz. The amplifiers were assembled on pallets and tested. A photograph of an amplifier pallet is shown in Fig. 8 and the measured gain of a typical amplifier is shown in Fig. 9. The assembled switch and amplifier are shown in the photographs of Figs. 10 and 11. The gain of the 3-stage amplifier with isolators is shown in Fig. 12.

D. 800 MHz SUBSYSTEM

The 800 MHz amplifier and switch were designed in a similar manner as the 4 GHz amplifiers. The solid-state devices used in this case were AT-41470 low-noise bipolar transistors. A photograph of the switch and amplifier is shown in Fig. 13 and 14. The gain response of the 2-stage amplifier is shown in Fig. 15.

E. ANTENNAS

Folded-dipole antennas were chosen for the radiometer since they can easily be made on a printed-circuit board, they can be made balanced, and they operate over a wide bandwidth.⁵ A

photograph of the 800 and 4000 MHz antenna assembly is shown in Fig. 16. Each antenna on the antenna board, also shown in Fig. 16, is connected to a 3.6mm coaxial line that protrudes out the back of the drawn-aluminum housing. The antenna board is mounted within the housing at a distance of 1.6mm from the open end. The 1.6mm gap is filled with a layer of neoprene rubber foam that acts as a thermal insulator. A 300K-ohm thermistor (Victory Engineering, Model 53A55) is epoxied into the antenna board so that it protrudes slightly through the foam rubber to contact the tissues being measured. The thermistor wires also come out the back of the aluminum housing.

The back of the aluminum housing also acts as the reflecting backplane for the 800 MHz antenna; a brass plate (38.1mm wide x 16.5mm high x 0.8mm thick) mounted on the coaxial line of the 4 GHz antenna at a distance of 10 cm from the rear of the antenna board acts as its reflecting backplane.

The VSWR of these antennas measured while the assembly is in contact with tissue is shown in Fig. 17.

F. LOW-FREQUENCY COMPONENTS

The schematic for the dual-frequency radiometer, including the low-frequency and digital components, is shown in Fig. 18. the low-frequency components consist of a 100 Hz modulator, a filter/amplifier, a synchronous detector and loop amplifier, a pulse-width modulator, and a switching regulator.

A photograph of the 100 Hz modulator and its associated schematic are shown in Figs. 19 and 20. This circuit produces a 200 Hz, crystal-controlled square-wave that is divided by a flip-

flop to achieve a 100 Hz modulation frequency. IC3 and Q5, and IC4 and Q6 produce 10 V pulses capable of driving 20 ma to the collector of each bipolar amplifier stage in the 800 MHz switch. Q3 and Q4 provide the same function for the 4000 MHz switch with 3 V pulses driving 10 ma to the drains of the FET amplifiers. Q1 and Q2 provide a slow-turn-on 3.6 V supply for Q3 and Q4.

The filter/amplifier is shown in the photograph of Fig. 21 and schematically in Fig. 22. All ICs are OP-27 low-noise operational amplifiers. The first stage is a buffer stage that provides AC coupling, transient protection, and a DC return path for the active filter. The second stage is the active filter with a gain and cutoff frequency of approximately 3 dB and 1 KHz.

The third stage is a variable-gain amplifier that provides 0 to 40 dB of gain. The filter response at full gain for the entire circuit is shown in Fig. 23.

The photograph and schematic for the synchronous detector and loop amplifier are shown in Figs. 24 and 25. The synchronous detector is built around the AD630 balanced modulator/demodulator chip, connected as an in-phase detector. In this mode the AD630 will produce a DC output voltage that is proportional to the difference between the two input signals when the two input signals are in phase with the reference signal, which in this case is the 100 Hz modulation to the switches. Therefore, any system noise that has been impressed on either or both inputs is greatly reduced and the overall detection sensitivity is greatly increased.

IC3 in Fig. 25 is the loop amplifier. The amplifier is an

integrator with a time constant of approximately 3 seconds. The op-amp is connected in the inverting mode so that when the input voltage goes negative (this is indicative of an increasing target temperature), the output goes positive. A change in the output voltage of the loop amplifier causes a change in the noise power out of the noise diode which in turn brings the input voltage to zero or into a balanced loop condition.

The pulse-width modulator board is shown in the photograph of Fig. 26 and schematically in Fig. 27. The CA1524 outputs 28 V pulses at a 1 KHz repetition rate to the diode noise source. The pulse width of these pulses varies between 0 and 100% as the control voltage varies between 1 and 3.5 V. The DC average of these pulses is proportional to the target temperature, and it is this voltage that is read by the microprocessor and converted into temperature.

Most of the DC voltages required by the various components in the radiometer system are supplied by the switching regulator shown in the photograph of Fig. 28 and the schematic of Fig. 29. The power supply was designed to operate with a +12 VDC input which would be supplied by a rechargeable battery in Phase II. The FET bias voltages, that is the -5 V gate supply and +3 V drain supply, are sequenced such that on turn-on the gate voltage is on before the drain voltage and on turn-off the gate is off after the drain voltage. The turn-on and turn-off sequencing can be seen in the oscillographs of Fig. 30a and b.

G. DIGITAL PROCESSOR SUBSYSTEM

The digital processor subsystem is shown in the photograph

FIGURE CAPTIONS

- Fig. 1. Temperature-versus-depth profile in tissue calculated using assumed arterial and ambient temperatures of 37 and 21°C. The tissue geometry is that of a body slice in the area of the appendix. TF(rad) is the radiometric temperature measured at a depth of 0 cm.
- Fig. 2. A 2.5 cm thick body slice in the area of the appendix (12 Processus vermiformis).
- Fig. 3. Temperature profile in tissue calculated using assumed arterial and ambient temperatures of 37 and 21°C. An elevated temperature of 2°C, representing an inflamed appendix, is calculated for depths of (a) 4 cm, (b) 6 cm, and (c) 8 cm.
- Fig. 4. The calculated radiometric temperature as a function of surface temperature and hot-spot depth for an 800 MHz radiometer.
- Fig. 5. The calculated radiometric temperature as a function of surface temperature and hot-spot depth for a 4 GHz radiometer.
- Fig. 6. Basic Dicke radiometer schematic.
- Fig. 7. Schematic of a single-pole-double-throw (SPDT) microwave switch using low-noise amplifiers.
- Fig. 8. Photograph of the NE13783-4 low-noise amplifier pallet.
- Fig. 9. Measured gain of a typical NE13783-4 amplifier pallet.
- Fig. 10. Photograph of the assembled FET SPDT switch.

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4. Dicke, RH, "The Measurement of Thermal Radiation at Microwave Frequencies," Rev. Scient. Instr., Vol. 17, pp 268-275, July 1946.
5. The Radio Amateur's Handbook, Goodman, B, editor, The American Radio League, Newington, CT, pp 389-392, 1967.


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01B1 27          DEC      R7
01B2 27          DEC      R7
01B3 F80B        LDI      0BH
01B5 5F          STR      R7
01B6 F8CB        LDI      0CBH
01B8 53          STR      R3
01B9 F8FC        LDI      0FCH
01BB 59          STR      R9
01BC F85E        LDI      5EH
01BE 54          STR      R4
01BF F801        LDI      01H
01C1 55          STR      R5
01C2 C00056      LBR      LP1
01C5 7B          SEQ      CHK2
01C6 DE          SEP      RE
01C7 27          DEC      R7
01C8 27          DEC      R7
01C9 27          DEC      R7
01CA F806        LDI      06H
01CC 5F          STR      R7
01CD F865        LDI      65H
01CF 53          STR      R3
01D0 F8CF        LDI      0CFH
01D2 59          STR      R9
01D3 F801        LDI      01H
01D5 55          STR      R5
01D6 F822        LDI      22H
01D8 54          STR      R4
01D9 C00056      LBR      LP1
01DC 60          EXDLY    IRX
01DD D0          DELAY    LDI      R0
01DE F8CF        LDI      0CFH
01E0 26          DEC      R6
01E1 56          STR      R6
01E2 26          DEC      R6
01E3 56          STR      R6
01E4 F801        LDI      PT1
01E6 F5          SD
01E7 56          STR      R6
01E8 60          IRX
01E9 F800        LDI      00H
01EB 75          SDB
01EC 56          STR      R6
01ED 32DC        BZ      EXDLY
01EF 26          DEC      R6
01F0 30E4        BR      PT1
01F2 DE          SEP      QUIT
01F3 DE          SEP      RE
01F4 C00000      LBR      START

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9 0175 57          STR      R7          ;STORE 2nd DIGIT IN R7-1
10 0176 6E          INP        6
11 0177 27          DEC      R7
12 0178 57          STR      R7          ;STORE LS DIGIT IN R7-1
13                ***DISPLAY DIGITS
14 0179 F84F        LDI      4FH          ;DISABLE CDP1885, ENABLE CDP1811
15 017A 26          DEC      R6
16 017C 56          STR      R6
17 017D F833        LDI      33H
18 017F 26          DEC      R6
19 0180 56          STR      R6
20 0181 F808        LDI      08H
21 0183 26          DEC      R6
22 0184 56          STR      R6
23 0185 61          OUT      1
24 0186 62          OUT      2
25 0187 62          OUT      2
26                ***
27 0188 07          LDN      R7          ;LOAD LS THRU MS DIGIT
28 0189 26          DEC      R6
29 018A 56          STR      R6
30 018B 17          INC      R7
31 018C 07          LDN      R7
32 018D 26          DEC      R6
33 018E 56          STR      R6
34 018F 17          INC      R7
35 0190 07          LDN      R7
36 0191 26          DEC      R6
37 0192 56          STR      R6
38 0193 64          OUT      4
39 0194 26          DEC      R6
40 0195 63          OUT      3
41 0196 64          OUT      4
42 0197 26          DEC      R6
43 0198 63          OUT      3
44 0199 64          OUT      4
45 019A 26          DEC      R6
46 019B 67          OUT      7
47 019C DE          SEP      RE          ;CALL DELAY
48                ***MAIN LOOP CNTR TEST
49 019D 0D          LDN      RD          ;LOAD CNTR & SUBTRACT 1
50 019E FF01        SMI      01H
51 01A0 32F2        BZ       QUIT        ;IF LOOP CNTR=0 THEN END
52 01A2 5D          STR      RD
53 01A3 FF01        SMI      01H
54 01A5 3A05        BNZ      CHK2        ;IF LOOP CNTR=1
55 01A7 F810        LDI      20H        ;SET MUX CHNL=2 & RETURN
56 01A9 5A          STR      RA
57 01AA F8A0        LDI      0A0H
58 01AC 5B          STR      RB
59 01AD F830        LDI      30H
60 01AF 5C          STR      RC
61 01B0 27          DEC      R7

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266 0139 07	LDR	R7	
267 013A 26	DEC	R6	
268 013B 56	STR	R6	
269 013C F864	LDR	64H	
270 013E 26	DEC	R6	
271 013F 56	STR	R6	
272 0140 F8FC	LDR	0FCH	
273 0142 26	DEC	R6	
274 0143 56	STR	R6	
275 0144 67	OUT	7	
276 0145 64	OUT	4	
277 0146 65	OUT	5	
278 0147 66	OUT	6	
279 0148 67	OUT	7	
280 0149 C4	NOP		
281 014A C4	NOP		
282 014B C4	NOP		
283 014C F8F0	LDR	0F0H	
284 014E 26	DEC	R6	
285 014F 56	STR	R6	
286 0150 67	OUT	7	
287 0151 6C	INP	4	
288 0152 6D	INP	5	
289 0153 17	INC	R7	
290 0154 57	STR	R7	#STORE MS DIGIT IN R7
291 0155 6E	INP	6	
292 0156 27	DEC	R7	
293 0157 57	STR	R7	#STORE REMAINDER IN R7-1
294 0158 F8F2	LDR	0F2H	#DIVIDE REMAINDER BY 10 (0FH)
295 015A 26	DEC	R6	
296 015B 56	STR	R6	
297 015C 07	LDR	R7	
298 015D 26	DEC	R6	
299 015E 56	STR	R6	
300 015F F80A	LDR	0AH	
301 0161 26	DEC	R6	
302 0162 56	STR	R6	
303 0163 F8FC	LDR	0FCH	
304 0165 26	DEC	R6	
305 0166 56	STR	R6	
306 0167 67	OUT	7	
307 0168 64	OUT	4	
308 0169 65	OUT	5	
309 016A 67	OUT	7	
310 016B C4	NOP		
311 016C C4	NOP		
312 016D C4	NOP		
313 016E F8F0	LDR	0F0H	
314 0170 26	DEC	R6	
315 0171 56	STR	R6	
316 0172 67	OUT	7	
317 0173 6C	INP	4	
318 0174 6D	INP	5	

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0213 00FC 09      LDN      R9
0214 00FD 26      DEC      R6
0215 00FE 56      STR      R6
0216 00FF F8F0    LDI      0F0H
0217 0101 26      DEC      R6
0218 0102 56      STR      R6
0219 0103 67      OUT      7
0220 0104 64      OUT      4
0221 0105 67      OUT      7
0222 0106 C4      NOP
0223 0107 C4      NOP
0224 0108 C4      NOP
0225 0109 F8F0    LDI      0F0H
0226 010B 26      DEC      R6
0227 010C 56      STR      R6
0228 010D 67      OUT      7
0229 010E 26      DEC      R6
0230 010F 6C      INP      4
0231 0110 6E      INP      6      #INPUT BYTE TO STACK
0232 0111 6D      INP      5
0233 0112 60      IRX
0234 0113 F800    LDI      00H      #COMPLEMENT IF NEG AT C1
0235 0115 56      STR      R6
0236 0116 26      DEC      R6
0237 0117 17      INC      R7
0238 0118 07      LDN      R7
0239 0119 FFFF    SMI      0FFH
0240 011B 27      DEC      R7
0241 011C 3A29    >      BNZ      C2
0242 011E F0      LDX
0243 011F FBFF    XRI      0FFH
0244 0121 FC01    ADI      01H
0245 0123 56      STR      R6
0246 0124 60      IRX
0247 0125 FBFF    LDI      0FFH
0248 0127 56      STR      R6
0249 0128 26      DEC      R6
0250 0129 04      C2      LDN      R4      #ADD CONSTANT
0251 012A F4      ADD
0252 012B 57      STR      R7
0253 012C 60      IRX
0254 012D 05      LDN      R5
0255 012E 74      ADC
0256 012F 17      INC      R7
0257 0130 57      STR      R7
0258      ***CONVERT TO DECIMAL DIGITS
0259 0131 F8F2    LDI      0F2H      #DIVIDE BY 100 (64H)
0260 0133 26      DEC      R6
0261 0134 56      STR      R6
0262 0135 07      LDN      R7
0263 0136 26      DEC      R6
0264 0137 56      STR      R6
0265 0138 27      DEC      R7

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00160 00BF 60          IRX
00161                ***CONVERT AVERAGE TO TEMPERATURE
00162 00C0 27          DEC      R7          #SUBTRACT CONSTANT FROM AVG.
00163 00C1 07          LDN      R7
00164 00C2 36          STR      R6
00165 00C3 03          LDN      R3
00166 00C4 F5          SD
00167 00C5 57          STR      R7
00168 00C6 17          INC      R7
00169 00C7 07          LDN      R7
00170 00C8 56          STR      R6
00171 00C9 0F          LDN      RF
00172 00CA 75          SDB
00173 00CB 57          STR      R7
00174 00CC 07          LDN      R7          #COMPLEMENT IF SUBTR. GOES NEG.
00175 00CD FFFF        SMI      OFFH
00176 00CF 3AD9        BNZ      C1
00177 00D1 27          DEC      R7
00178 00D2 07          LDN      R7
00179 00D3 FBFF        XRI      OFFH
00180 00D5 FC01        ADI      01H
00181 00D7 57          STR      R7
00182 00D8 17          INC      R7
00183 00D9 FBFC        LDI      0FCH          #DISABLE CDP1851, ENABLE CDP1853,
00184 00DB 26          DEC      R6          #& INITIALIZE
00185 00DC 56          STR      R6
00186 00DD F800        LDI      00H
00187 00DF 26          DEC      R6
00188 00E0 56          STR      R6
00189 00E1 61          OUT      1
00190 00E2 67          OUT      7
00191 00E3 FBFB        LDI      0F9H
00192 00E5 26          DEC      R6
00193 00E6 56          STR      R6
00194 00E7 27          DEC      R7
00195 00E8 07          LDN      R7          #LOAD X & Z REGS. & MULT. BY 93 (5DH)
00196 00E9 26          DEC      R6
00197 00EA 56          STR      R6
00198 00EB FB5D        LDI      5DH
00199 00ED 26          DEC      R6
00200 00EE 56          STR      R6
00201 00EF 64          OUT      4
00202 00F0 65          OUT      5
00203 00F1 67          OUT      7
00204 00F2 C4          NOP
00205 00F3 C4          NOP
00206 00F4 C4          NOP
00207 00F5 6C          INP      4
00208 00F6 6D          INP      5
00209 00F7 6E          INP      6
00210 00F8 FBFB        LDI      0F2H          #LOAD X REG. & DIVIDE BY CONSTANT
00211 00FA 26          DEC      R6
00212 00FB 56          STR      R6

```

```

00107 0082 FA0F      ANI      0FH      #MASK OUT BITS 5-6
00108 0084 57        STR      R7
00109 0085 0C        LDN      RC      #GIVE TOGGLE COMMAND
00110 0086 FF10      SMI      10H
00111 0088 26        DEC      R6
00112 0089 56        STR      R6
00113 008A 0C        LDN      RC
00114 008B 26        DEC      R6
00115 008C 56        STR      R6
00116 008D 64        OUT      4
00117 008E 64        OUT      4
00118 008F 6E        INF      6      #INPUT A-TO-D BITS 5,6,7,8,9,10,11,12
00119 0090 60        IRX
00120 0091 F4        ADD
00121 0092 56        STR      R6      #ADD PRESENT READING TO PREVIOUS
00122 0093 60        IRX
00123 0094 07        LDN      R7
00124 0095 74        ADC
00125 0096 56        STR      R6
00126 0097 26        DEC      R6
00127 0098 08        LDN      R8      #SUBTRACT 01H FROM LOOP COUNTER (R6)
00128 0099 FF01      SMI      01H
00129 009B 32A1      >      BZ      DIVN      #CHECK IF 16 RINGS HAVE BEEN TAKEN
00130 009D 58        STR      R8
00131 009E C0006E    >      LBR      AVG
00132
00133 00A1 F0        >      ***      LDX      #DIVIDE SUM OF 16 NOS. BY 16
00134 00A2 F6        DIVN
00135 00A3 F6        SHR
00136 00A4 F6        SHR
00137 00A5 F6        SHR
00138 00A6 56        STR      R6
00139 00A7 60        IRX
00140 00A8 F0        LDX
00141 00A9 FE        SHL
00142 00AA FE        SHL
00143 00AB FE        SHL
00144 00AC FE        SHL
00145 00AD 26        DEC      R6
00146 00AE F1        OR
00147 00AF FBFF      XRI      0FFH      #COMPLEMENT LS BYTE
00148 00B1 27        DEC      R7
00149 00B2 57        STR      R7
00150 00B3 17        INC      R7
00151 00B4 60        IRX
00152 00B5 F0        LDX
00153 00B6 F6        SHR
00154 00B7 F6        SHR
00155 00B8 F6        SHR
00156 00B9 F6        SHR
00157 00BA FBFF      XRI      0FFH      #COMPLEMENT MS BYTE
00158 00BC FA0F      ANI      0FH      #MASK OUT MS BITS
00159 00BE 57        STR      R7

```

```

00054 0048 F801      LDI      01H
00055 004A 55        STR      R5
00056 004B F812      LDI      12H
00057 004D 53        STR      R3
00058                ***BEGIN MEASUREMENT LOOP
00059 004E 7A        REQ      #SET RF SWITCHES TO 4GHZ
00060 004F F801      LDI      01H      #SET RETURN ADDRESS
00061 0051 BE        PHI      RE
00062 0052 F8DE      LDI      0DEH
00063 0054 AE        PLO      RE
00064 0055 DE        SEP      RE      #CALL DELAY SUBR.
00065                ***
00066 0056 F84F      LP1      LDI      4FH      #ENABLE CDP1851
00067 0058 26        DEC      R6      #SET PORT B TO INPUT
00068 0059 56        STR      R6      #SET PORT A TO OUTPUT
00069 005A F833      LDI      33H
00070 005C 26        DEC      R6
00071 005D 56        STR      R6
00072 005E F808      LDI      08H
00073 0060 26        DEC      R6
00074 0061 56        STR      R6
00075 0062 61        OUT      1
00076 0063 62        OUT      2
00077 0064 62        OUT      2
00078                ***
00079 0065 F800      LDI      00H      #INITIALIZE STACK TO 0
00080 0067 26        DEC      R6
00081 0068 56        STR      R6
00082 0069 26        DEC      R6
00083 006A 56        STR      R6
00084 006B F810      LDI      10H      #INITIALIZE R8 TO 16
00085 006D 58        STR      R8
00086                ***
00087 006E 0C        LDN      RC      #SET CD4066 INPUT MUX TO
00088 006F FF10      SMI      10H      #INPUT CHANNEL 1 OR 2,
00089 0071 26        DEC      R6      #GIVE A-TO-D CONVERT COMMAND,
00090 0072 56        STR      R6      #RESET CD4013 TOGGLE FF
00091 0073 0C        LDN      RC      #GIVE TOGGLE COMMAND TO
00092 0074 26        DEC      R6      #CD4013 TOGGLE FF
00093 0075 56        STR      R6
00094 0076 08        LDN      RB
00095 0077 26        DEC      R6
00096 0078 56        STR      R6
00097 0079 0A        LDN      RA
00098 007A 26        DEC      R6
00099 007B 56        STR      R6
00100 007C 64        OUT      4
00101 007D 64        OUT      4
00102 007E 64        OUT      4
00103 007F 64        OUT      4
00104                ***
00105 0080 26        DEC      R6      #INPUT A-TO-D BITS 5,6,7,8,1,2,3,4
00106 0081 6E        INP      6      #LSB=BIT 1, LSB=BIT 12

```

```

00001          ;**INITIALIZE REGISTERS          *****PROGRAM BOB*****
00002 0000 F84F      START      LDI      4FH      ;SET MS BYTE OF RAM TO 4FH
00003 0002 B3        PHI      R3
00004 0003 B4        PHI      R4
00005 0004 B5        PHI      R5
00006 0005 B6        PHI      R6
00007 0006 B7        PHI      R7
00008 0007 B8        PHI      R8
00009 0008 B9        PHI      R9
00010 0009 BA        PHI      RA
00011 000A BB        PHI      RB
00012 000B BC        PHI      RC
00013 000C BD        PHI      RD
00014 000D BF        PHI      RF
00015 000E F880      LDI      80H      ;R6 ADDRESS=4F80H <<STACK>>
00016 0010 A6        FLO      R6
00017 0011 E6        SEX      R6      ;SET STACK TO R6
00018 0012 F810      LDI      10H      ;R7 ADDRESS=4F10H <<TEMP. DATA>>
00019 0014 A7        FLO      R7
00020 0015 F800      LDI      00H      ;R8 ADDRESS=4F00H <<AVG. LOOP CNTR.>>
00021 0017 A8        FLO      R8
00022 0018 F820      LDI      20H      ;RA ADDRESS=4F20H <<MUX CHNL COMMAND>>
00023 001A AA        FLO      RA
00024 001B F830      LDI      30H      ;RB ADDRESS=4F30H <<CONVERT COMMAND>>
00025 001D AB        FLO      RB
00026 001E F840      LDI      40H      ;RC ADDRESS=4F40H <<TOGGLE COMMAND>>
00027 0020 AC        FLO      RC
00028 0021 F850      LDI      50H      ;RD ADDRESS=4F50H <<MAIN LOOP CNTR>>
00029 0023 AD        FLO      RD
00030 0024 F860      LDI      60H      ;RF ADDRESS=4F60H <<MATH CONSTANT>>
00031 0026 AF        FLO      RF
00032 0027 F861      LDI      61H      ;R9 ADDRESS=4F61H <<MATH CONSTANT>>
00033 0029 A9        FLO      R9
00034 002A F862      LDI      62H      ;R5 ADDRESS=4F62H <<MATH CONSTANT>>
00035 002C AS        FLO      R5
00036 002D F863      LDI      63H      ;R4 ADDRESS=4F63H <<MATH CONSTANT>>
00037 002F A4        FLO      R4
00038 0030 F864      LDI      64H      ;R3 ADDRESS=4F64H <<MATH CONSTANT>>
00039 0032 A3        FLO      R3
00040 0033 F800      LDI      00H      ;INITIALIZE RA TO MUX CHNL 1
00041 0035 5A        STR      RA
00042 0036 F880      LDI      80H      ;INITIALIZE CONVERT COMMAND
00043 0038 5B        STR      RB
00044 0039 F810      LDI      10H      ;INITIALIZE TOGGLE COMMAND
00045 003B 5C        STR      RC
00046 003C F803      LDI      03H      ;INITIALIZE MAIN LOOP CNTR TO 3
00047 003E 5D        STR      RD
00048 003F F807      LDI      07H
00049 0041 5F        STR      RF
00050 0042 F89E      LDI      9EH
00051 0044 59        STR      R9
00052 0045 F810      LDI      10H
00053 0047 54        STR      R4

```


J. PLANS FOR PHASE-II

The prototype unit will be delivered under Phase II of the program. A photograph of the shell of the planned prototype is shown in Fig. 38. Not shown in the photograph is the 12 volt, 3 amp-hour battery and charger unit that will connect to the pistol grip.

The display on the rear panel of the unit is a 16-character liquid-crystal display that will simultaneously display the three temperatures corresponding to the temperature of the surface and the temperature at two depths.

	<u>4 GHz</u> HEX (Decimal)	<u>800 MHz</u> HEX (Decimal)	<u>Thermistor</u> HEX (Decimal)
C1	64 (100)	64 (100)	64 (100)
C2	959 (2393)	A77 (2679)	BF5 (3100)
C3	73 (115)	BE (190)	F1 (241)
C4	140 (320)	140 (320)	12B (299)

For the above constants, the 800 MHz radiometer will resolve temperatures between 18.5 and 45.4°C; the 4 GHz radiometer between 9.8 and 54.1°C; and the thermistor between 19.3 and 40.4°C.

I. RADIOMETER EVALUATION

$$\text{Next Significant Digit (NSD)} = \frac{R1}{10} = D2+R2$$

$$\text{Least Significant Digit (LSD)} = R2.$$

D1, D2 and R2 are then displayed on the liquid crystal display.

The Q lines are next set to switch the latching switches into the 800 MHz position; and, with different constants in eqn. 2, a new temperature is measured and displayed. Finally the surface thermistor is interfaced to the A-to-D through a buffer amplifier and the multiplexer, and the surface temperature is calculated and displayed in a similar manner. The flow chart for the above sequence is shown in Fig. 36.

The source file that contains the assembly code for the radiometer system is listed in Appendix A.

H. BREADBOARD

The breadboard unit is shown in Fig. 37. The unit was calibrated by placing the antenna in contact with saline that was maintained at various temperatures. The antenna housing was covered with a thin layer of plastic food wrap for the calibration procedure. The saline was contained in a galvanized steel pail whose inside surfaces were lined with a 1/4 inch thick carbon-impregnated foam material. The lossy foam essentially makes the pail of saline appear as an infinite volume at a known temperature.

The radiometer and thermistor voltages were recorded for saline temperatures of 24 and 40°C. The constants of the linearizing equation (eqn. 2) are:

of Fig. 31. It consists of a power supply (± 15 V and +5 V), a CDP18S601 microboard computer, a multiply/divide unit, and an interface and display board.

The CDP18S601 card contains a CDP1802 CPU, a 2 MHz crystal-controlled clock, read-write memory, parallel I/O ports, and sockets for up to 8 kilobytes of EPROM. The layout of the major components on this card is shown in Fig. 32. The CDP1855 multiply/divide unit is located between the CDP18S601 and the interface card. The schematic for this device is shown in Fig. 33. The schematic for the interface and display card is shown in Fig. 34, and the respective card interconnection diagram is shown in Fig. 35.

The subsystem operation is basically as follows: On start-up, the CPU resets the Q line (P1-6) which sets the latching switches (see Fig. 18) to the 4 GHz radiometer position. The radiometer output voltage is connected to the 12-bit A-to-D converter on the interface card through a buffer amplifier and the input multiplexer. The CPU converts the 12-bit digital code into a temperature using

$$2) \quad T = \frac{C1*(N-C2)}{C3} + C4$$

where N = 12-bit digital number in hexadecimal and $C1$ through $C4$ are constants. The temperature, T , calculated in eqn. 2 is in hexadecimal and must be converted to decimal digits for display. This is accomplished by using the following

$$3) \quad \text{Most Significant Digit (MSD)} = \frac{T}{100} = \text{DIGIT 1}(D1) + \text{Remainder 1}(R1)$$

- Fig. 11. Photograph of the 3-stage FET amplifier.
- Fig. 12. Measured gain response of the 3-stage FET amplifier.
- Fig. 13. Photograph of the AT-41470 SPDT switch.
- Fig. 14. Photograph of the 2-stage AT-41470 amplifier.
- Fig. 15. Measured gain response of the 2-stage AT-41470 amplifier.
- Fig. 16. Photograph of the dual-frequency antenna assembly.
The printed circuit board with the 800 and 4000 MHz antennas is shown in the foreground.
- Fig. 17. a) VSWR of the 800 MHz antenna measured with the antenna in contact with body tissue; b) the same for the 4 GHz antenna.
- Fig. 18. Schematic representation of the dual-frequency radiometer.
- Fig. 19. Photograph of the 100 Hz modulator board.
- Fig. 20. Schematic diagram for the 100 Hz modulator.
- Fig. 21. Photograph of the 1 KHz filter/amplifier.
- Fig. 22. Schematic diagram for the 1 KHz filter/amplifier.
- Fig. 23. The gain response of the filter/amplifier as a function of frequency. (The gain is adjusted for a maximum.)
- Fig. 24. Photograph of the synchronous detector and loop amplifier board.
- Fig. 25. Schematic diagram for the synchronous detector and loop amplifier.
- Fig. 26. Photograph of the pulse-width modulator board.
- Fig. 27. Schematic diagram for the pulse-width modulator.
- Fig. 28. Photograph of the switching regulator.
- Fig. 29. Schematic diagram for the switching regulator.

PROG/ME/RAD3

1:43pm FEB. 24 1984

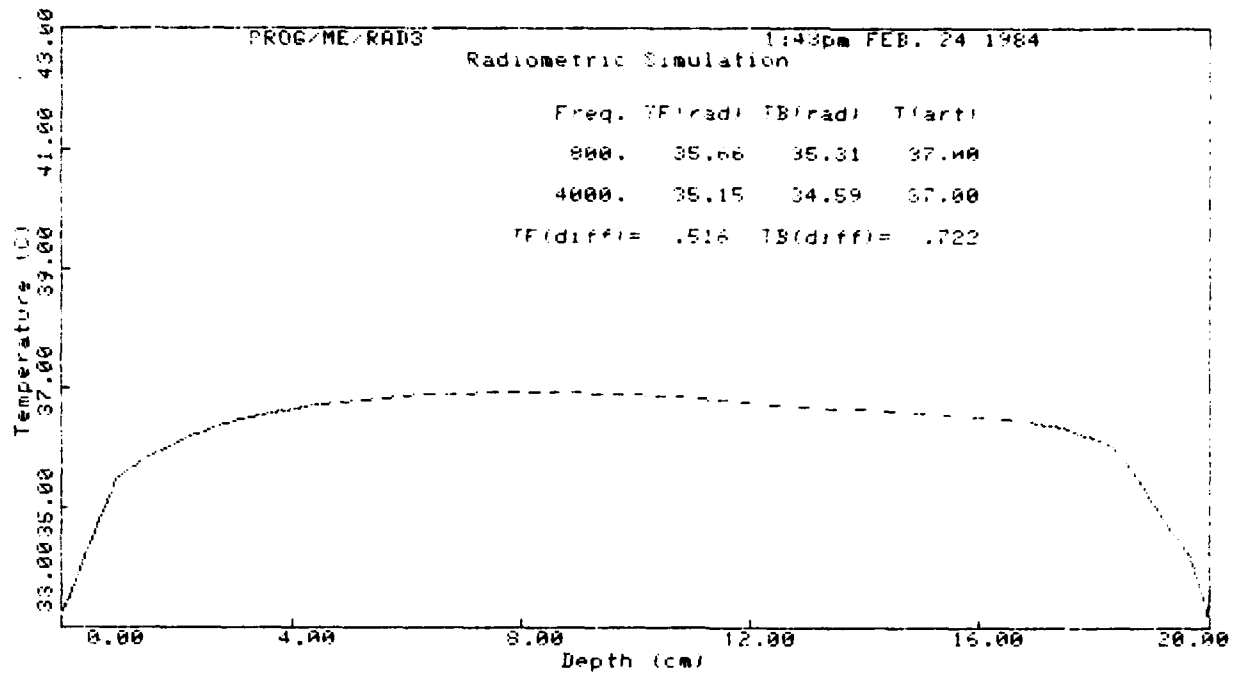
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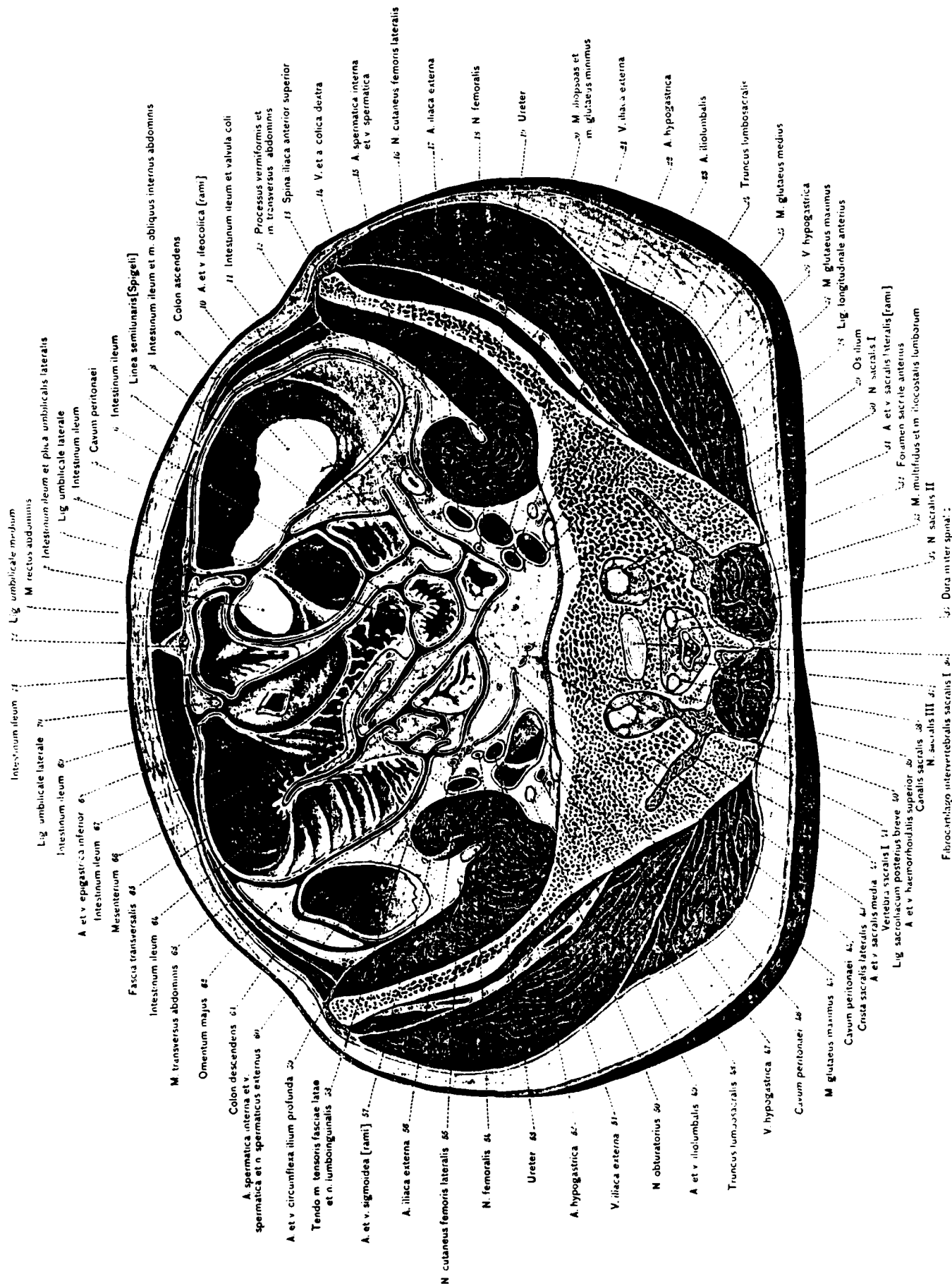
Freq. TF(rad) TB(rad) T(art)

800. 35.66 35.31 37.00

4000. 35.15 34.59 37.00

TF(diff)= .516 TB(diff)= .722





PROG/ME/RAD3

1309pm FEB. 24 1984

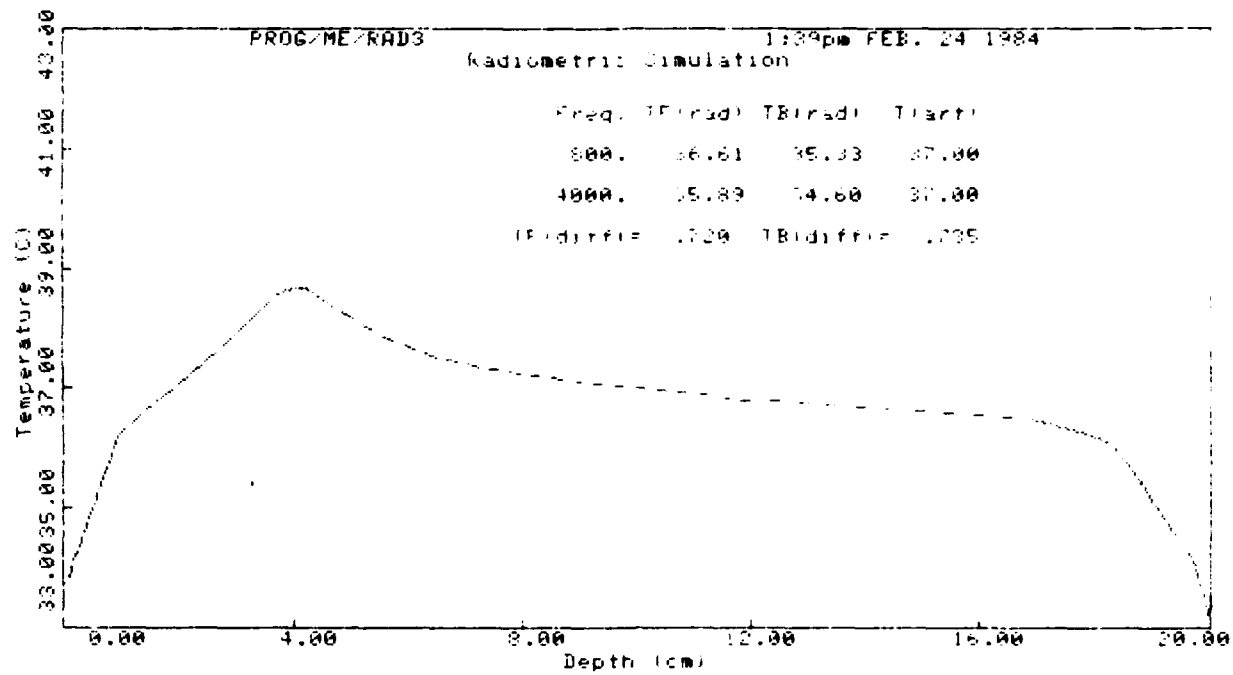
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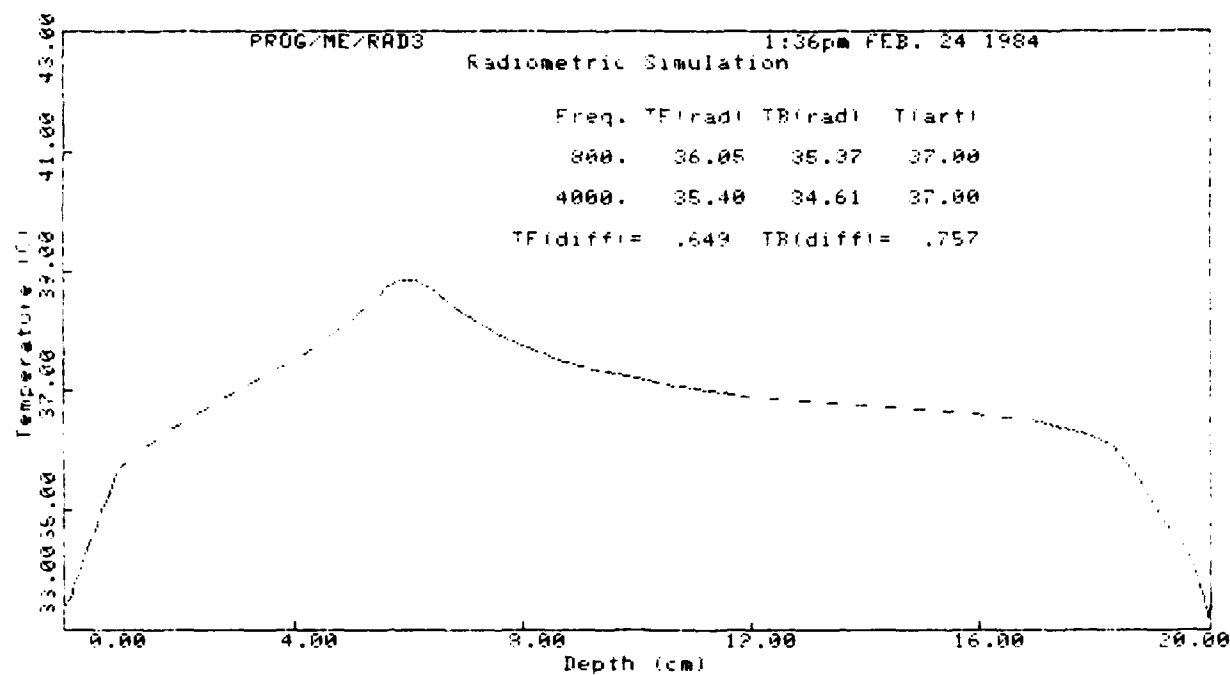
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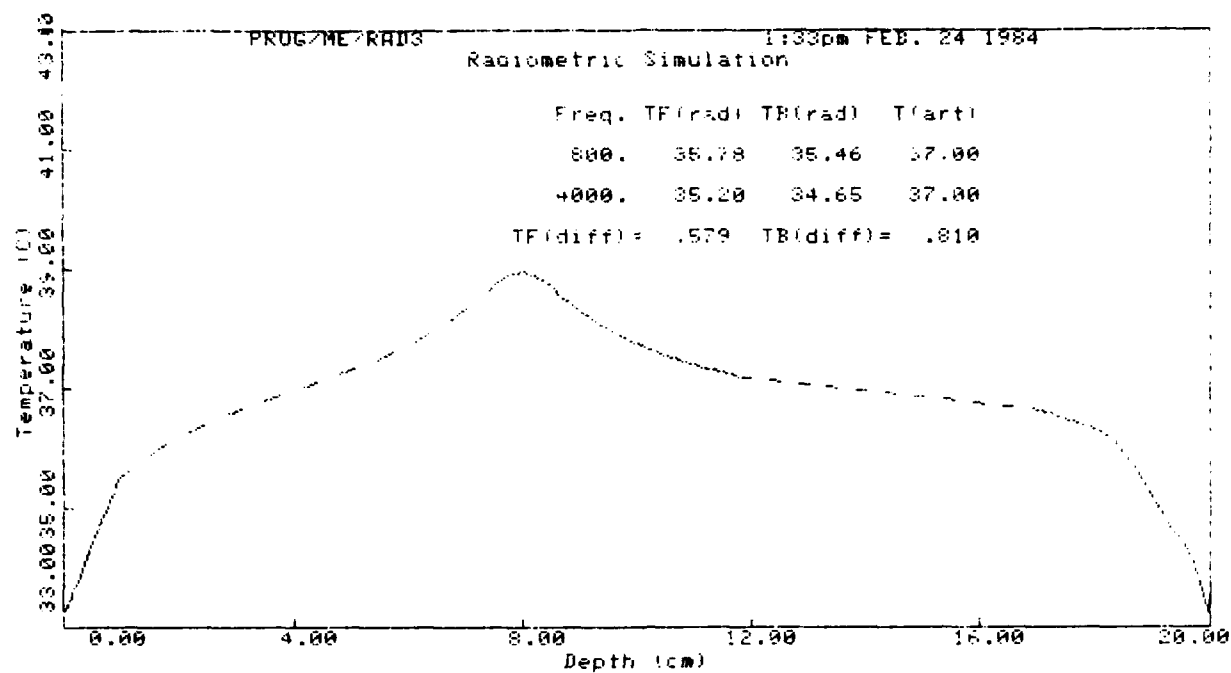
800. 36.61 35.33 37.00

4000. 35.89 34.60 37.00

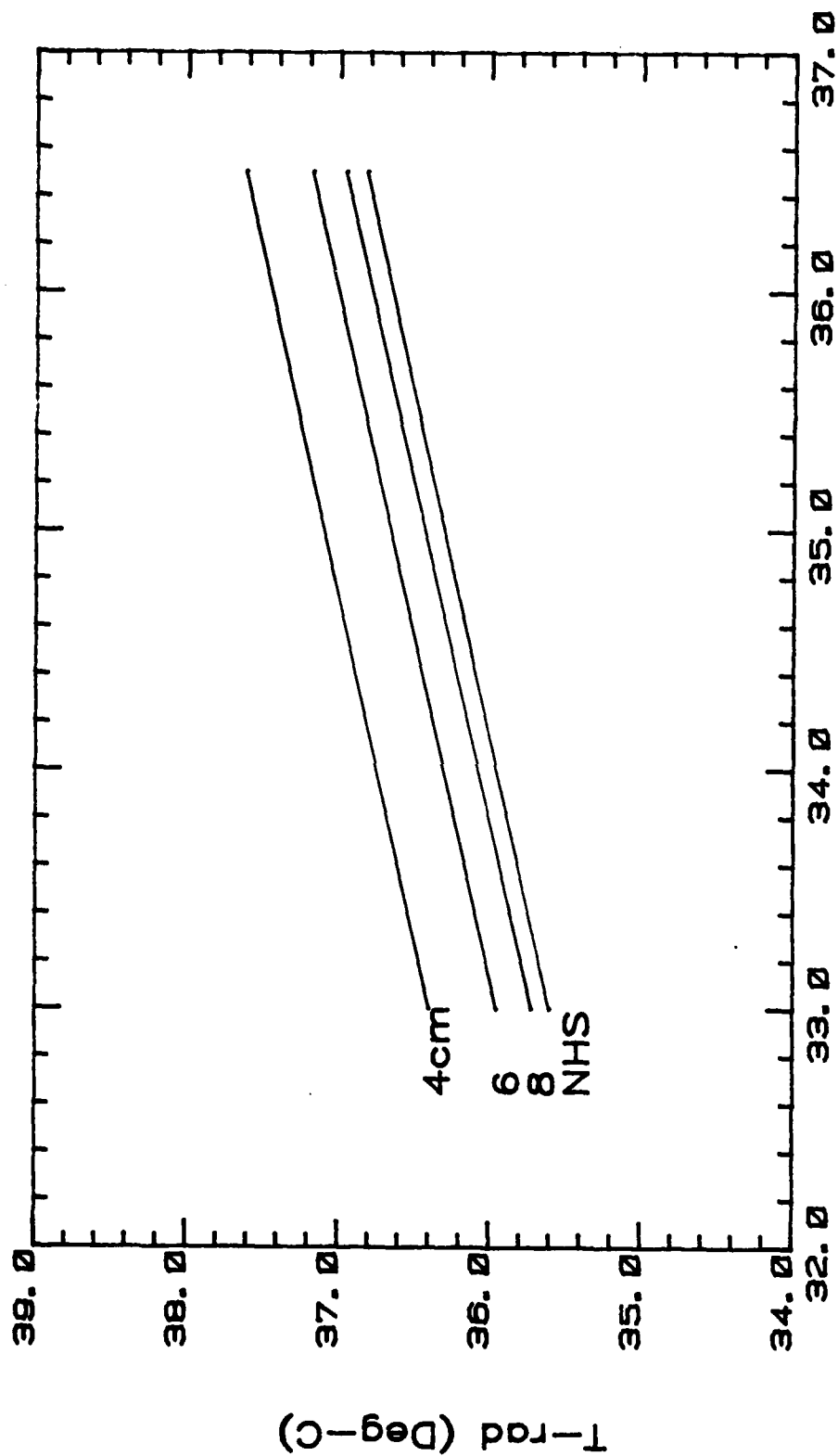
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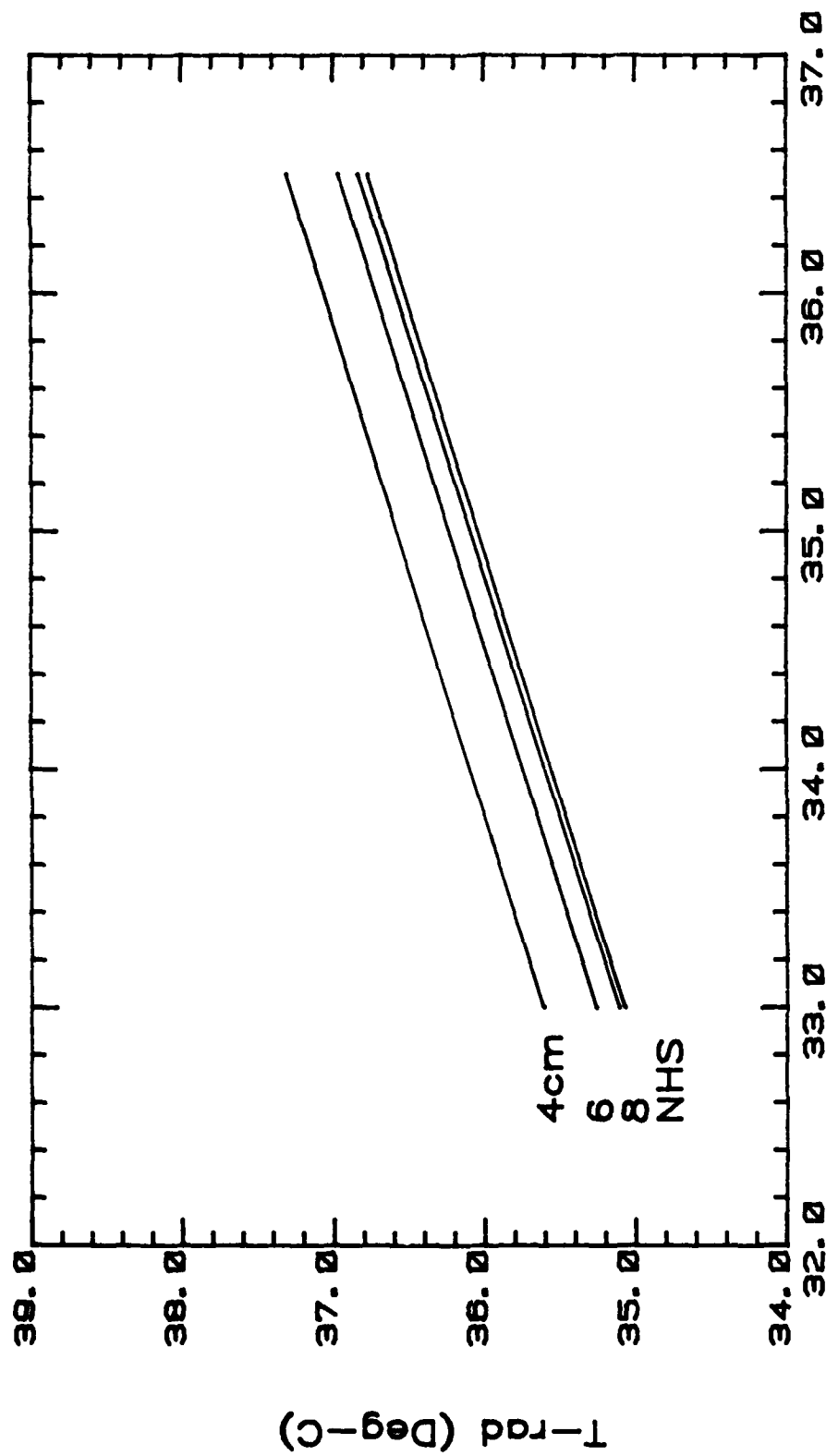
800 MHz Radiometer Simulation



NOVA

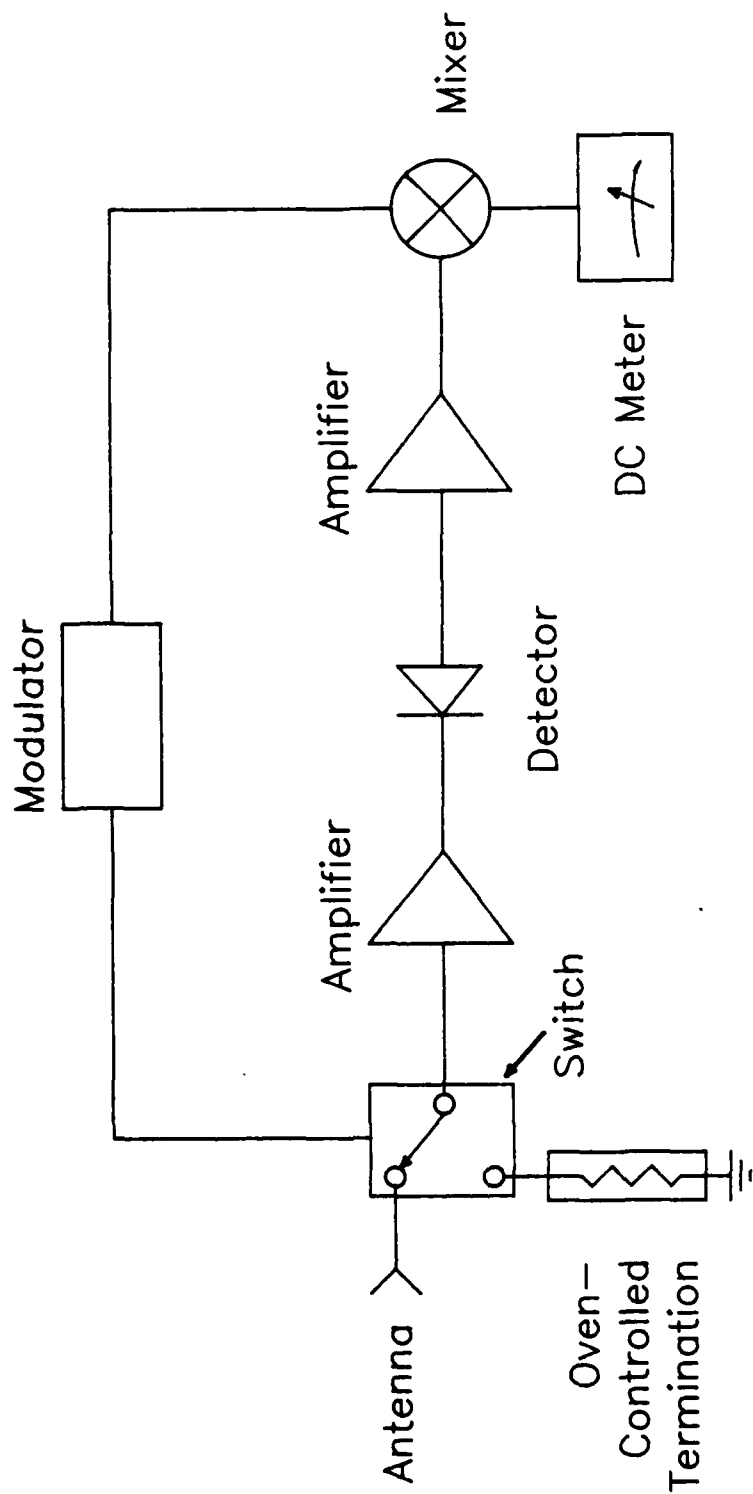
T-surf (Deg-C)

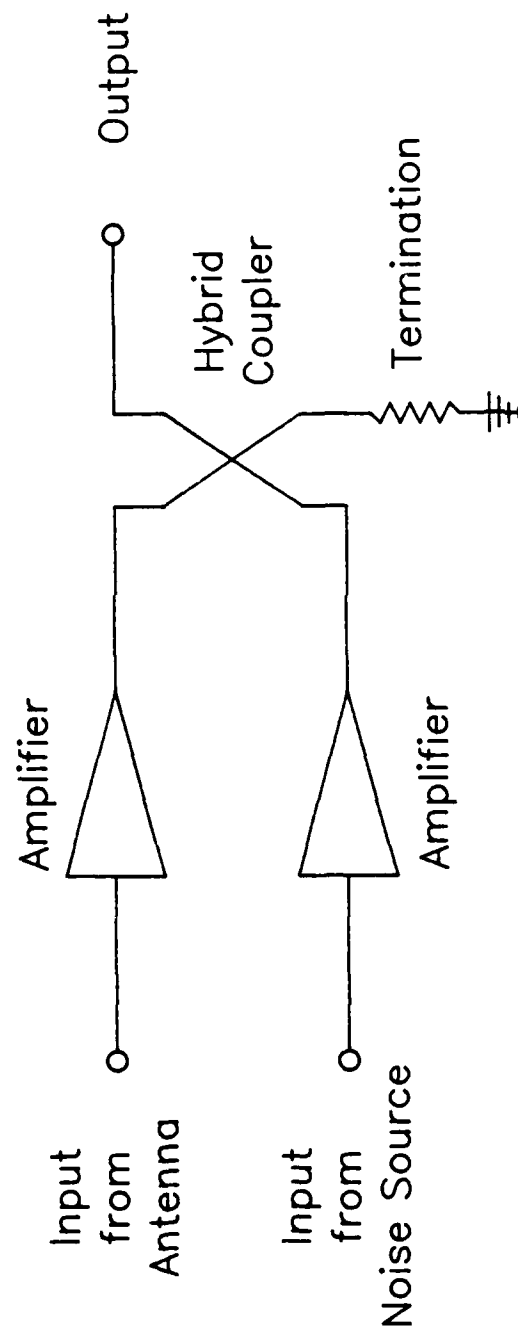
4000 MHz Radiometer Simulation

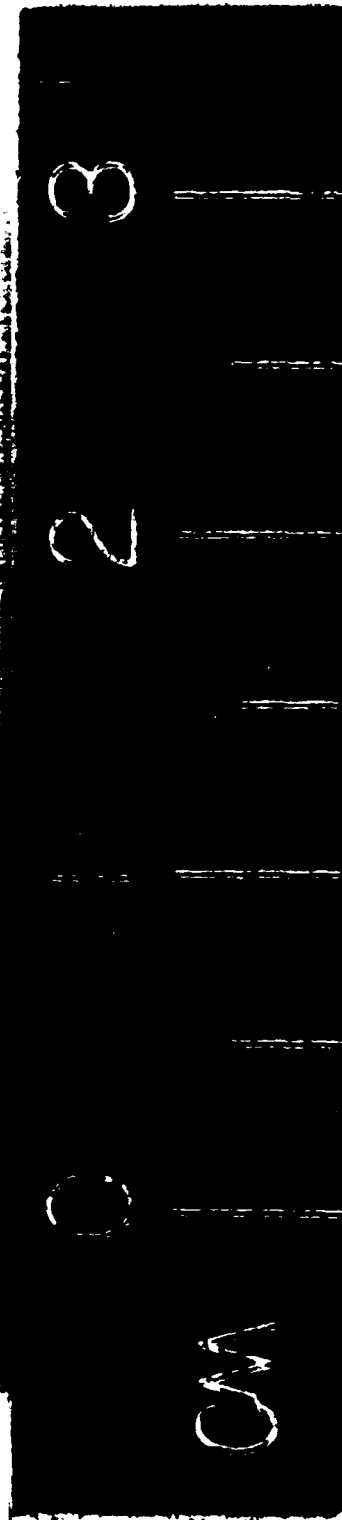
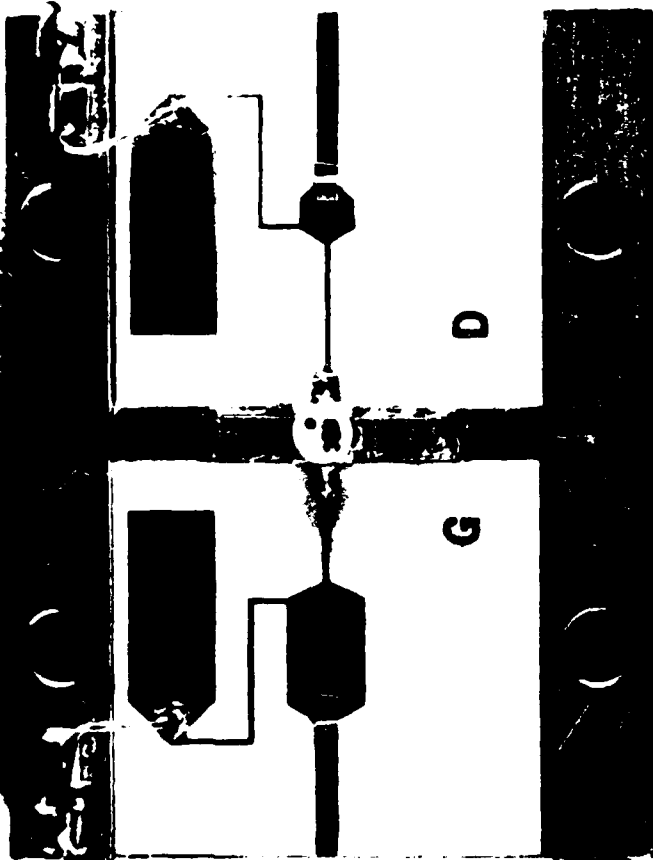


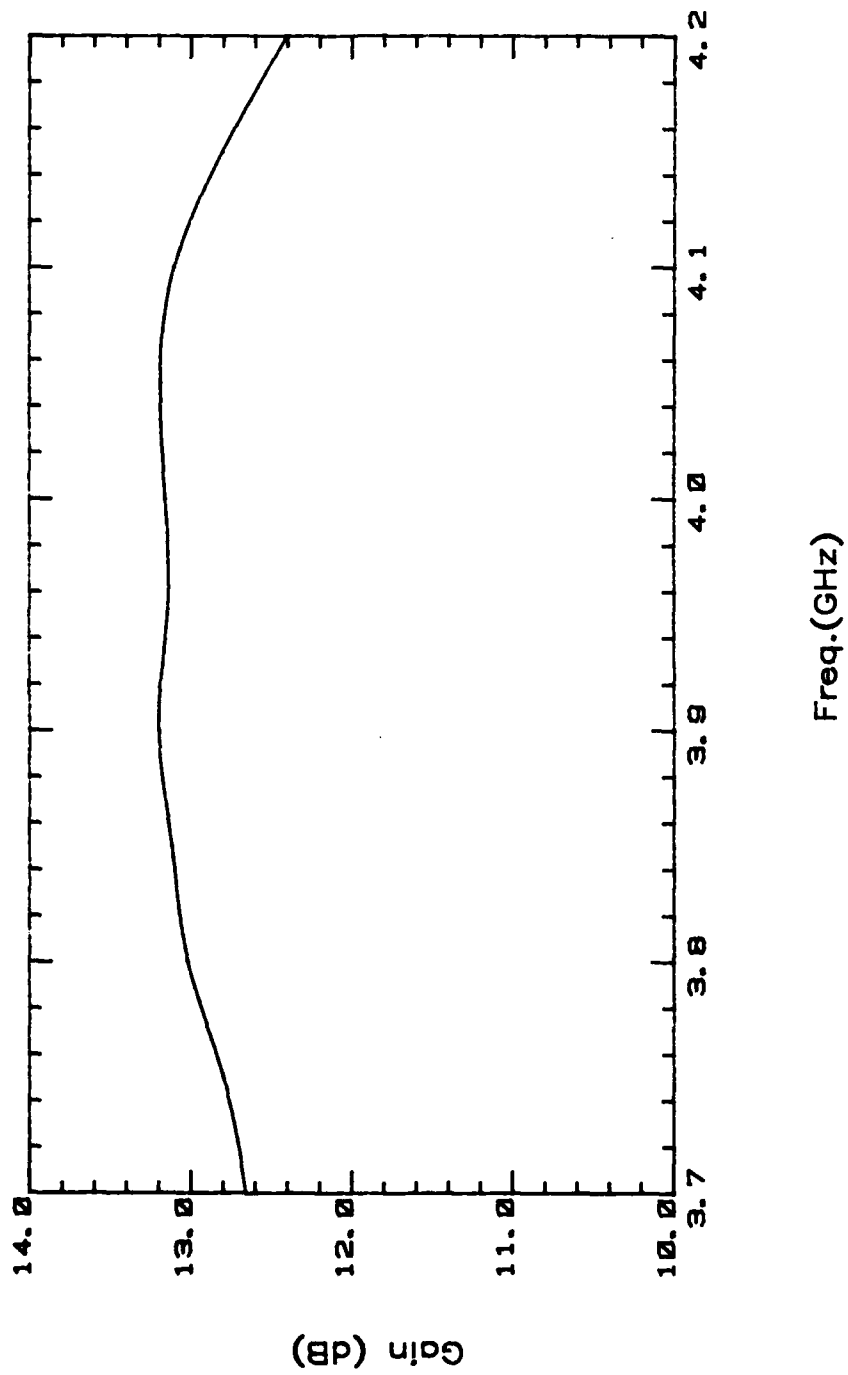
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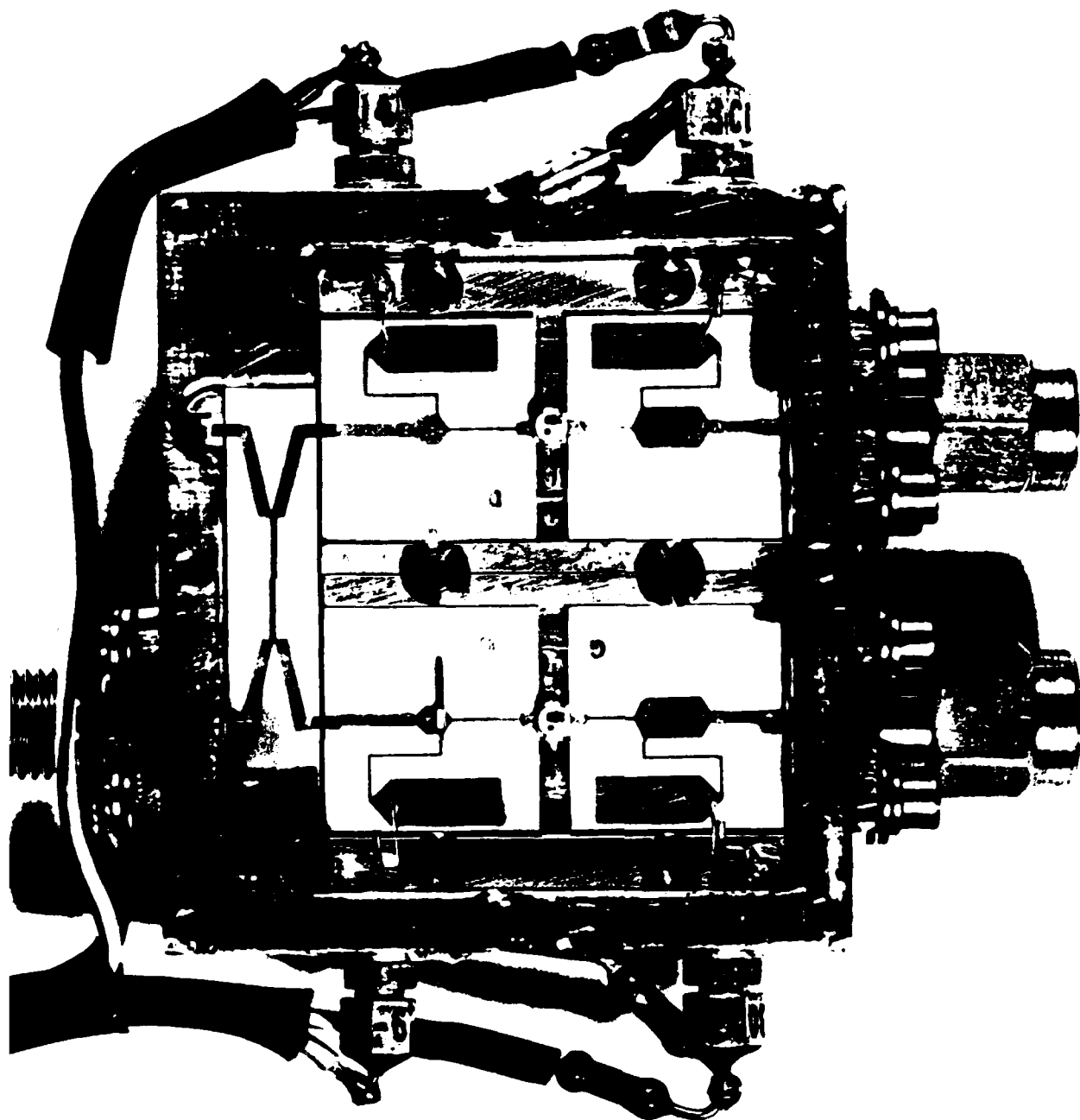
REDA

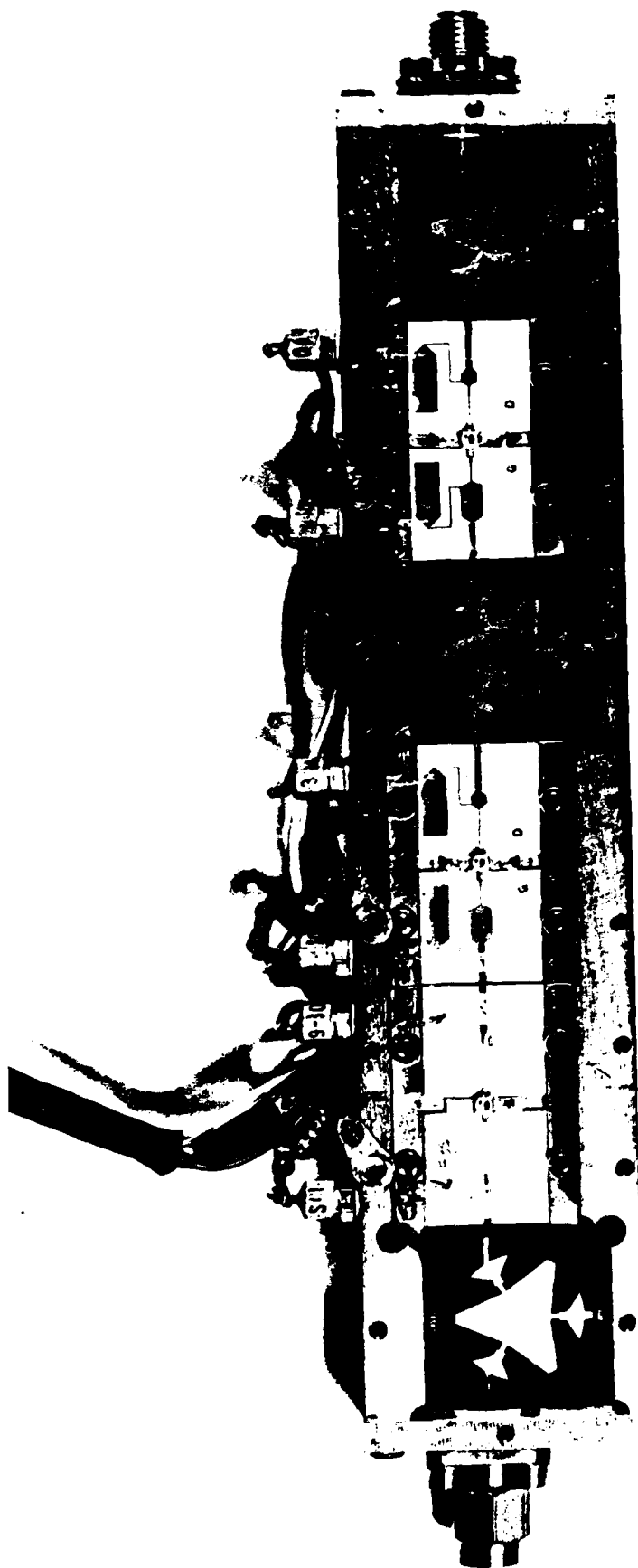


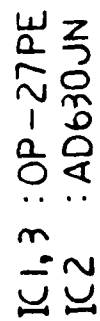




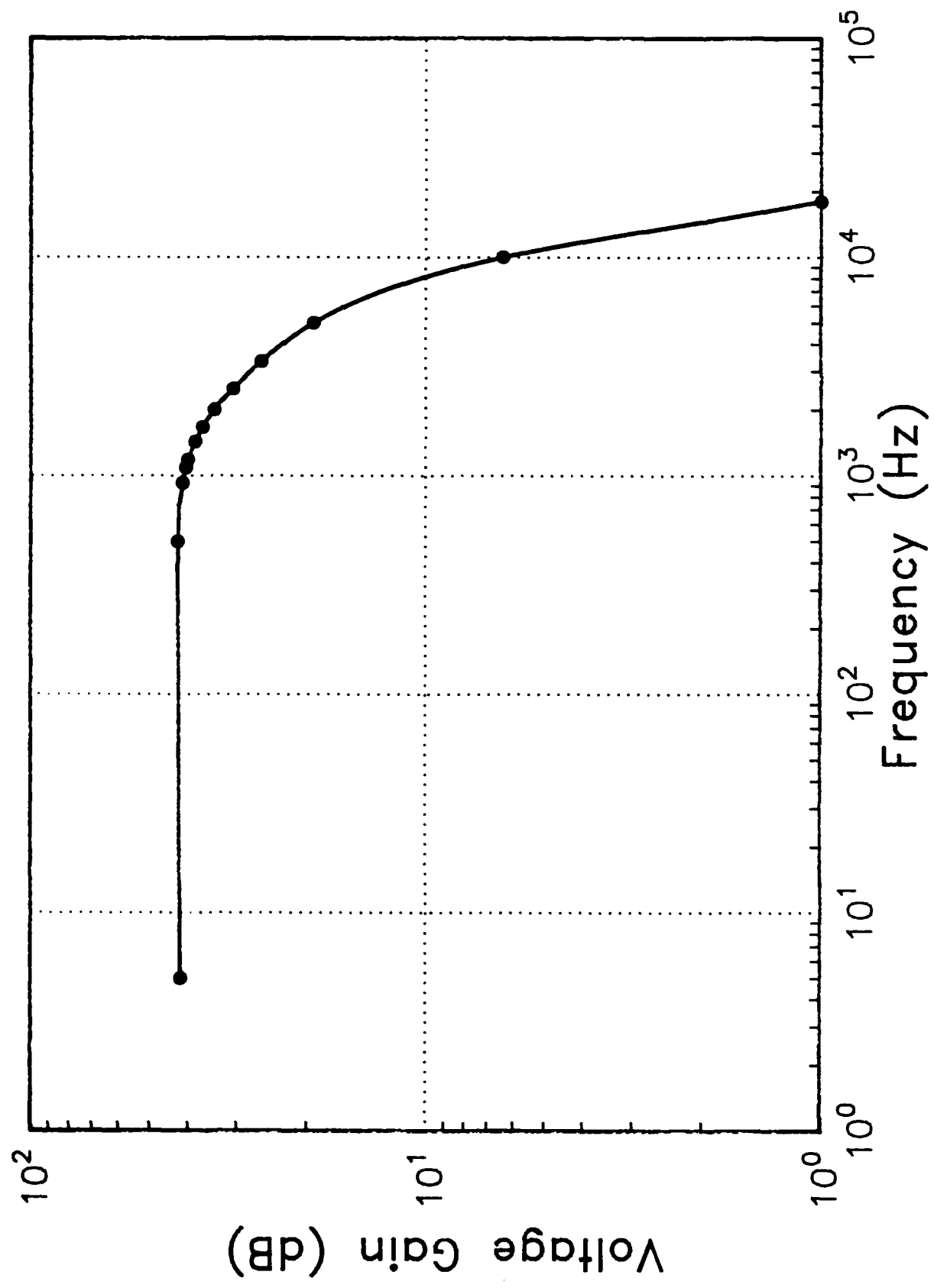




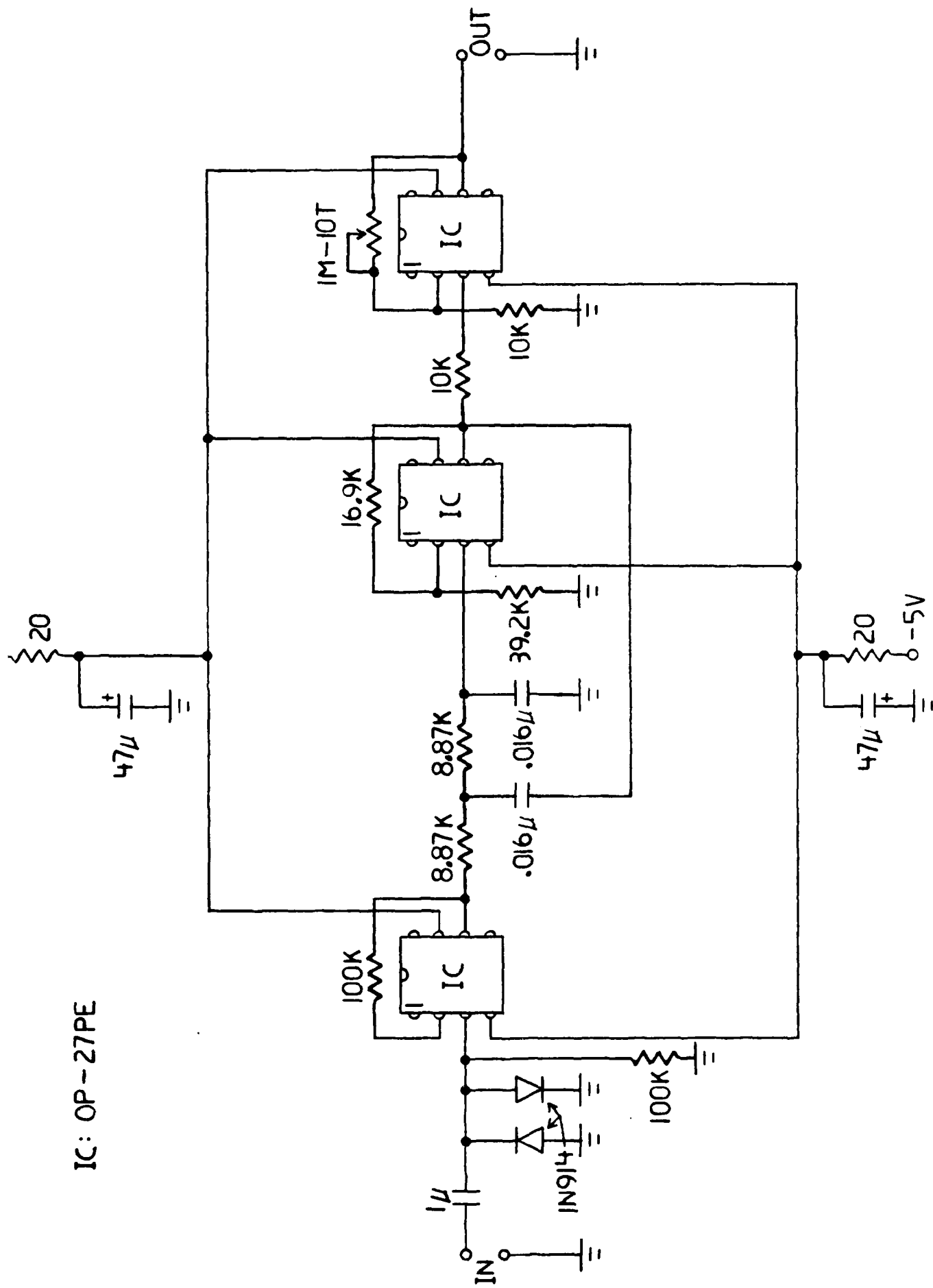


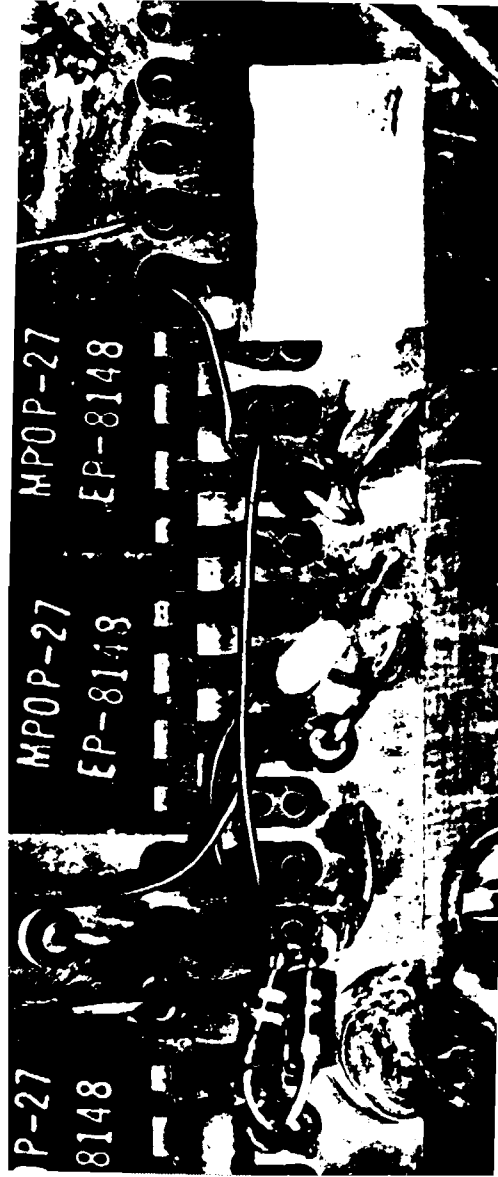


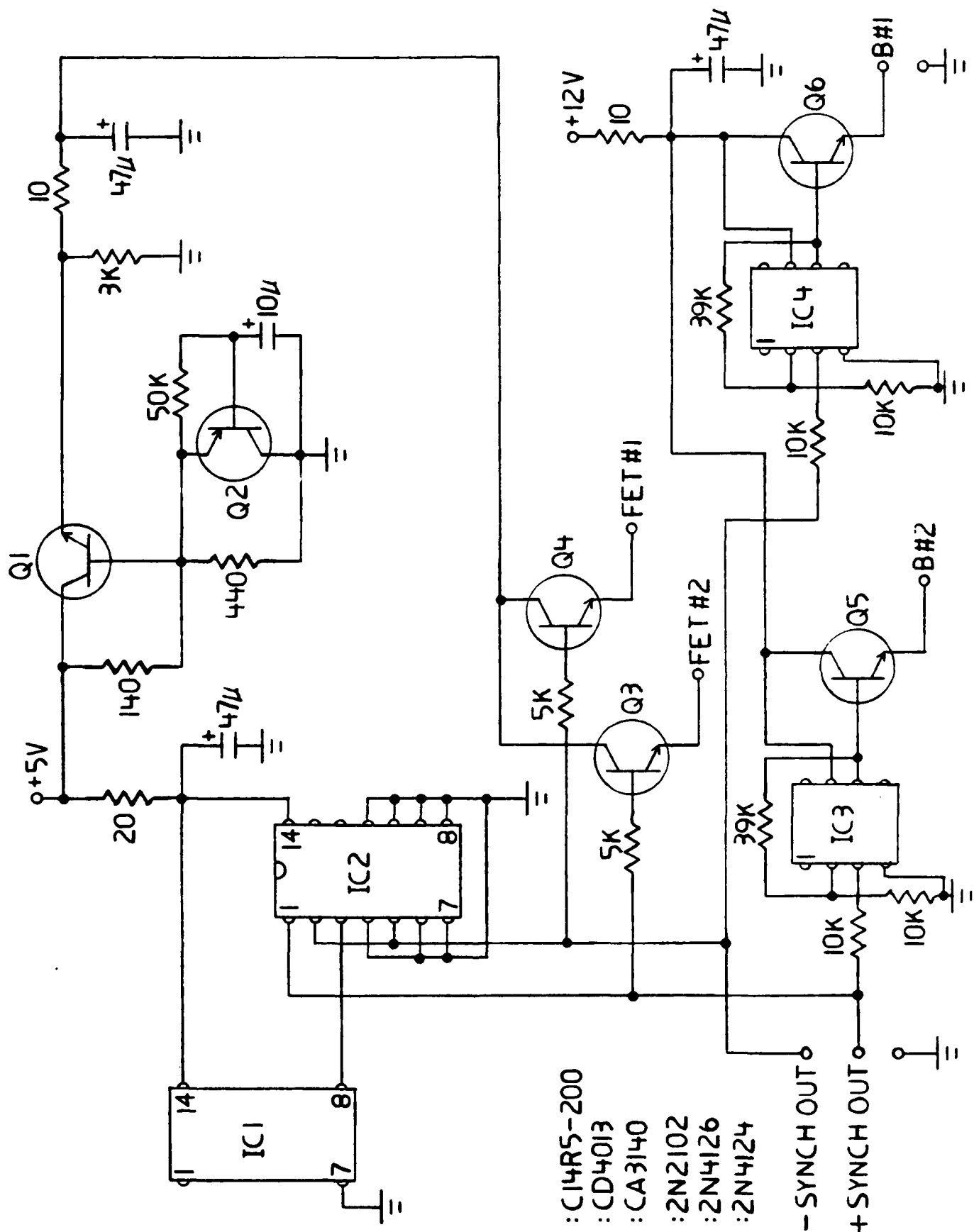




IC: OP-27PE

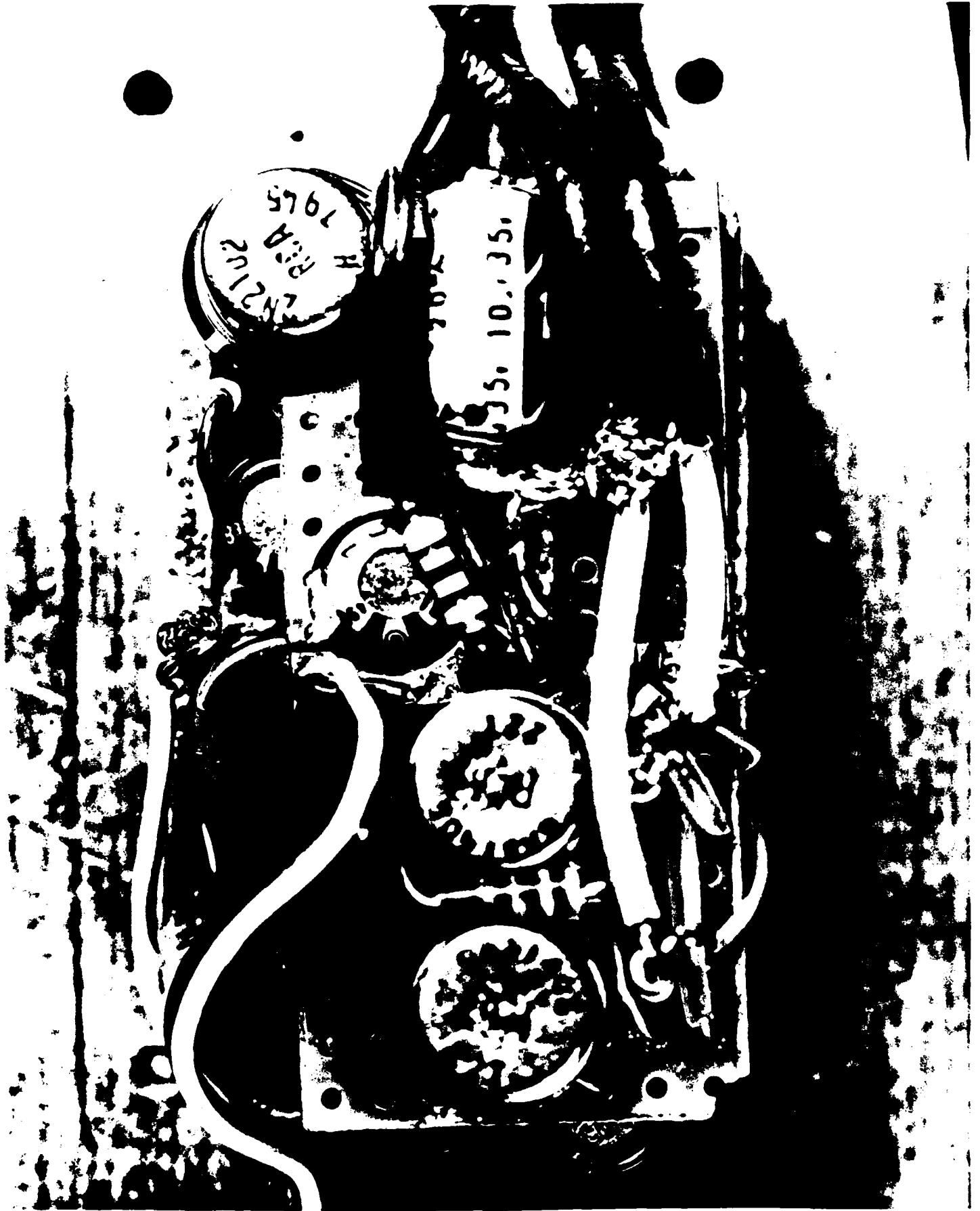




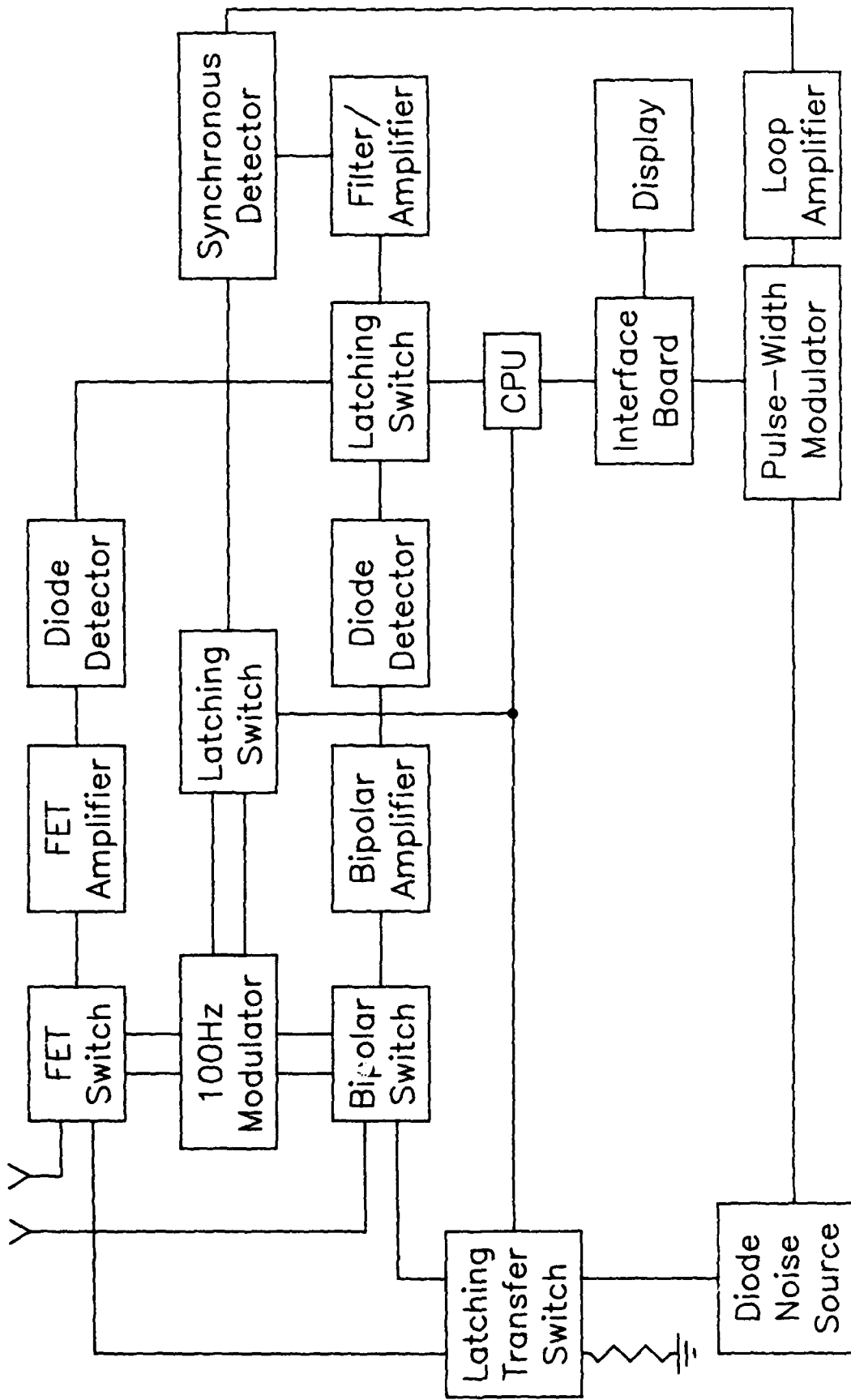


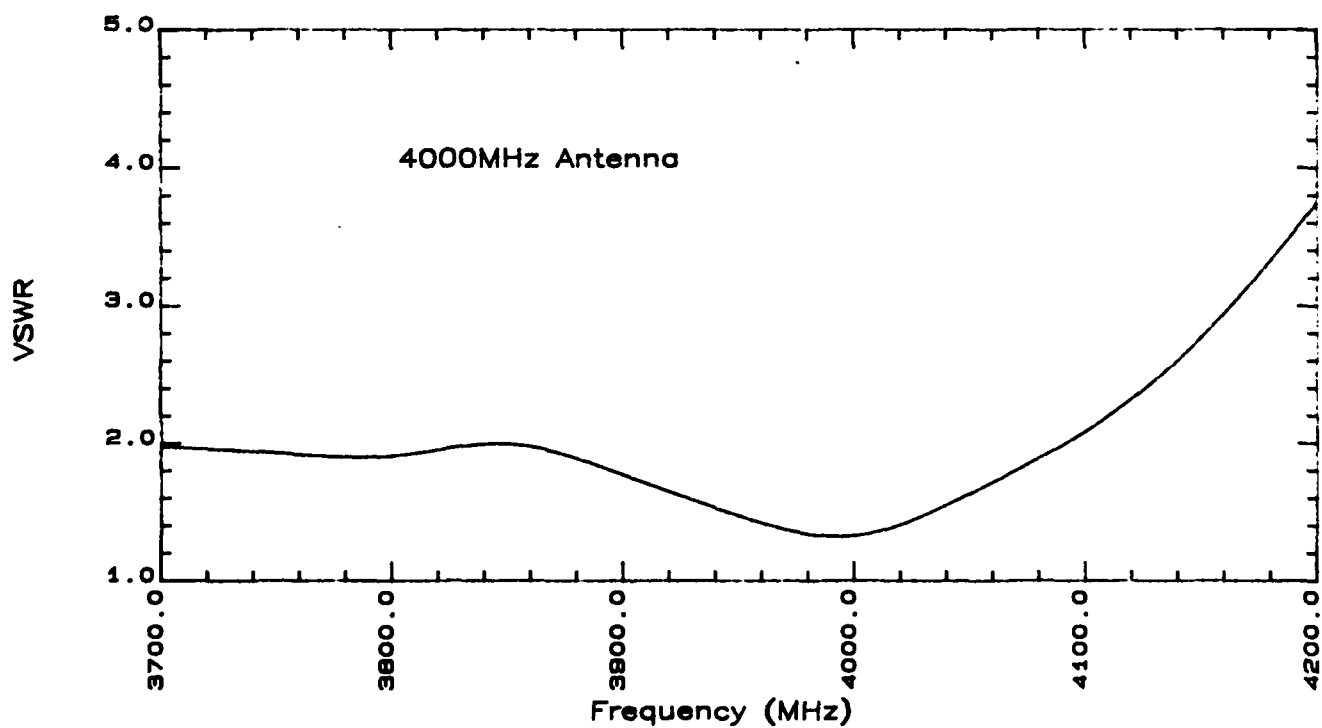
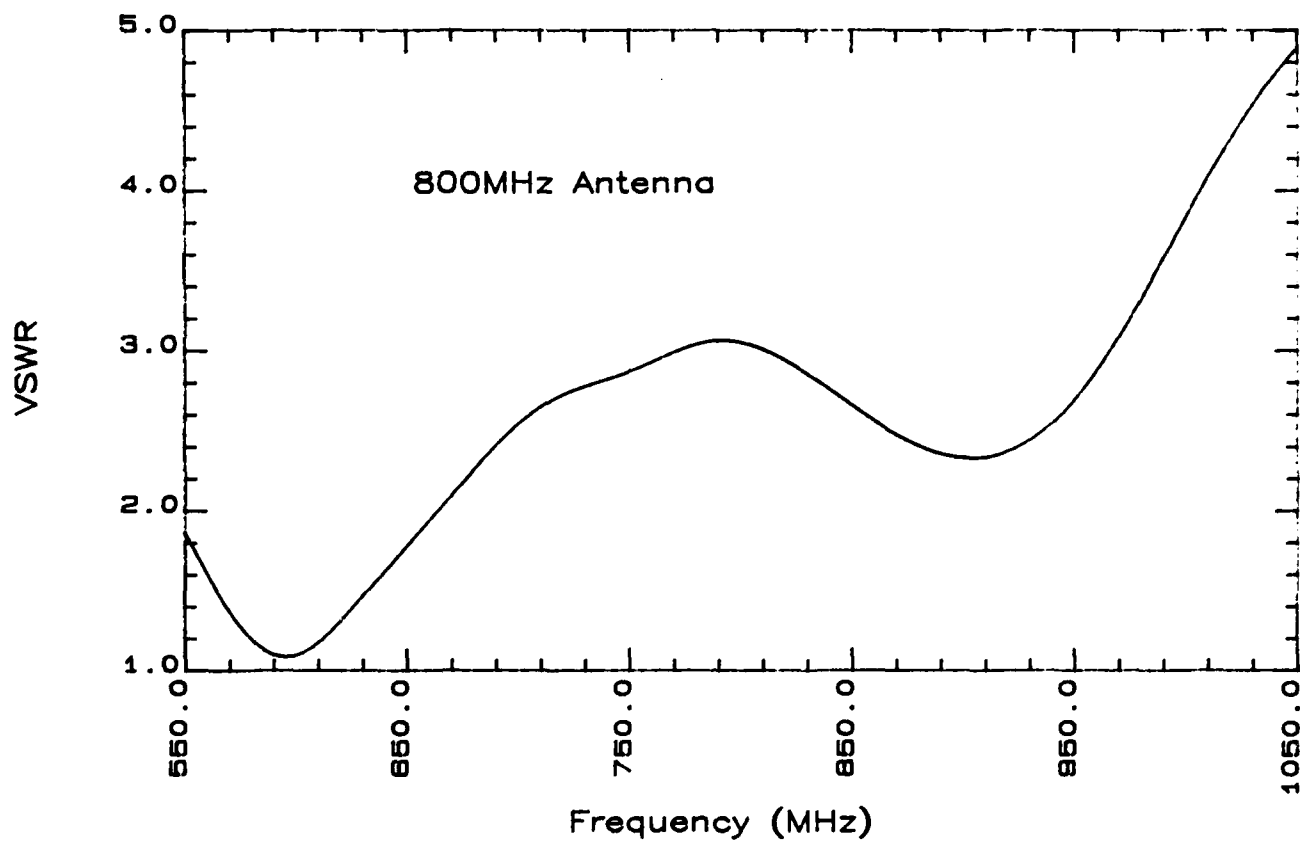
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 IC2 : CD4013
 IC3,4 : CA3140
 Q1 : 2N2102
 Q2 : 2N4126
 Q3-6 : 2N4124

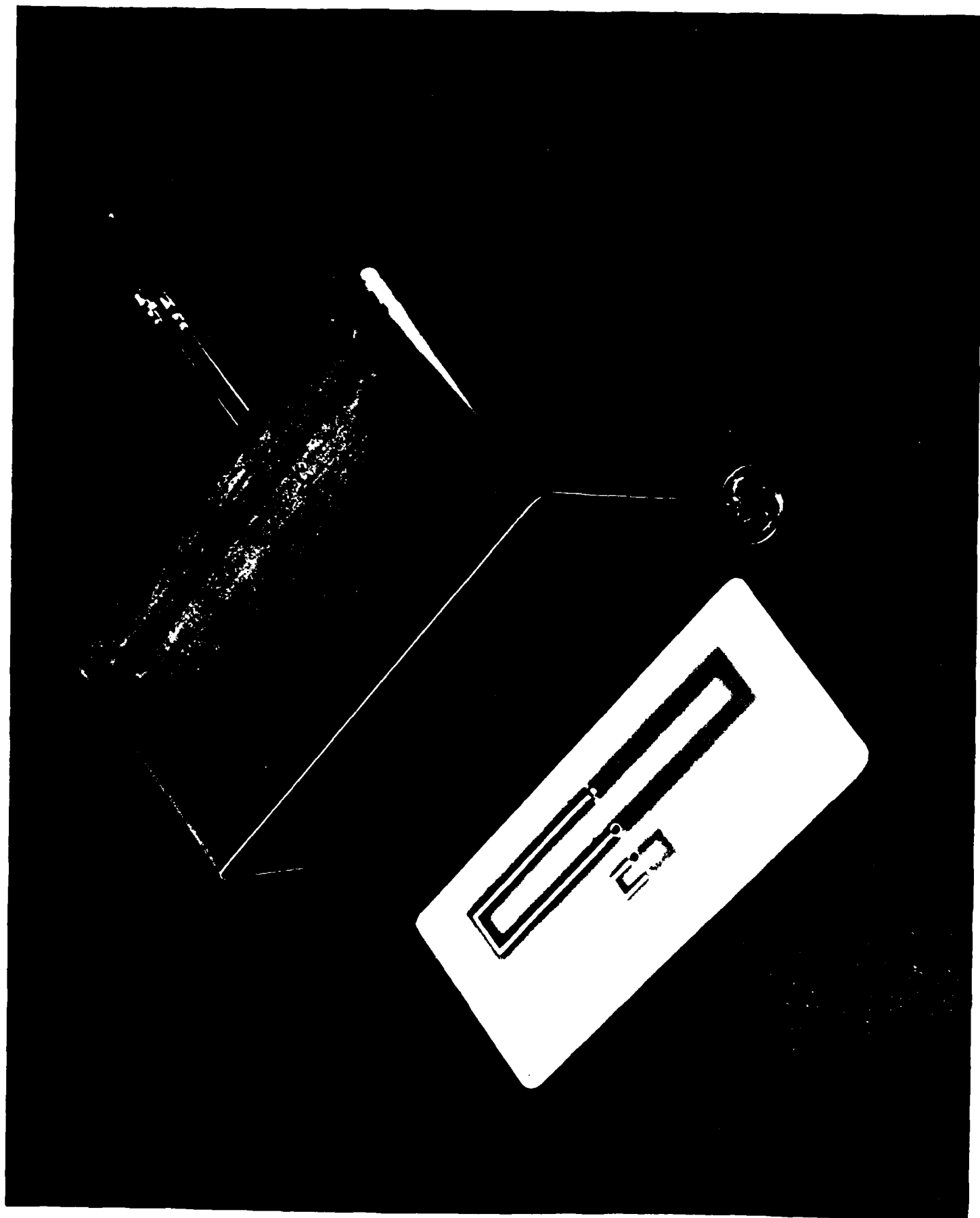
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 + SYNCH OUT

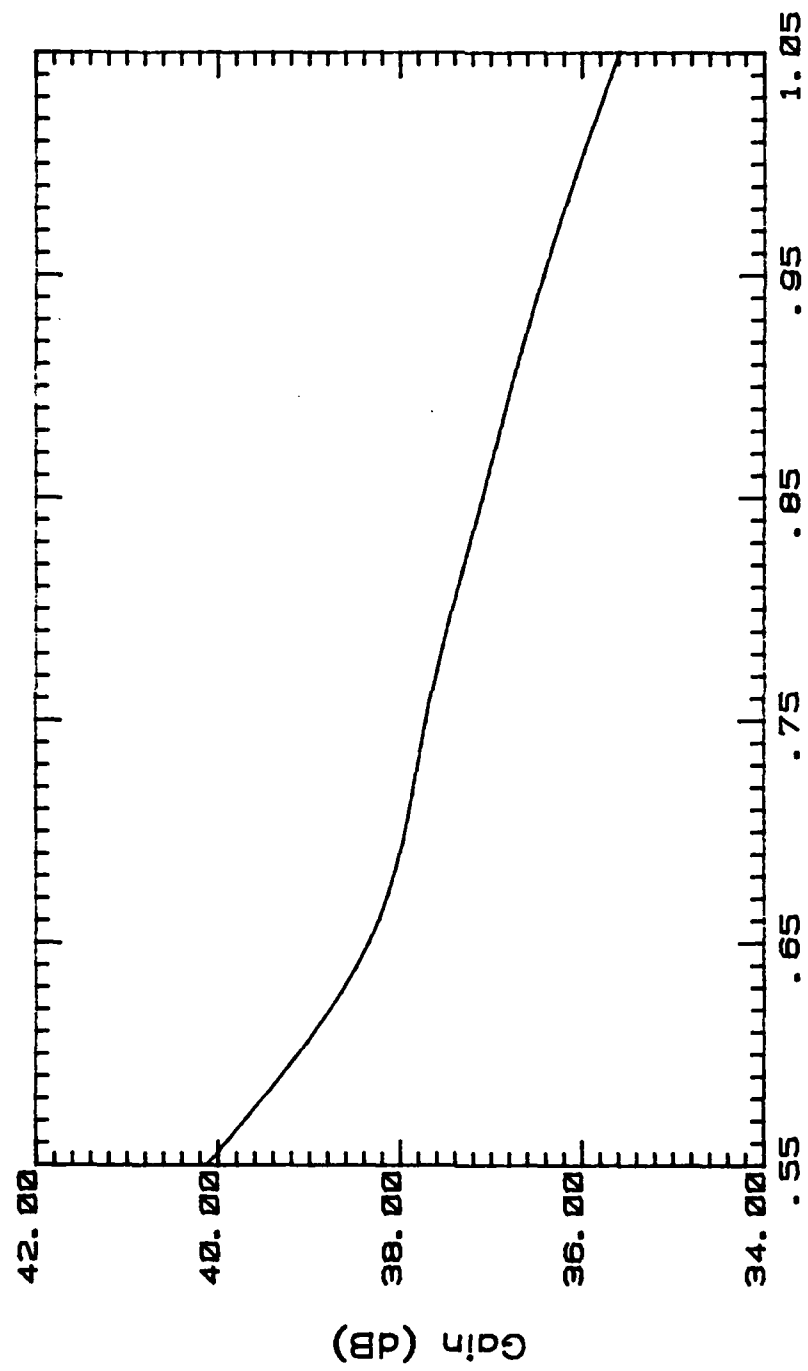


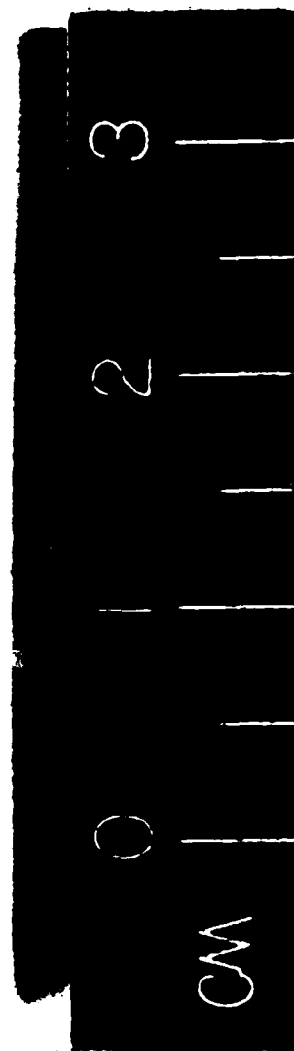
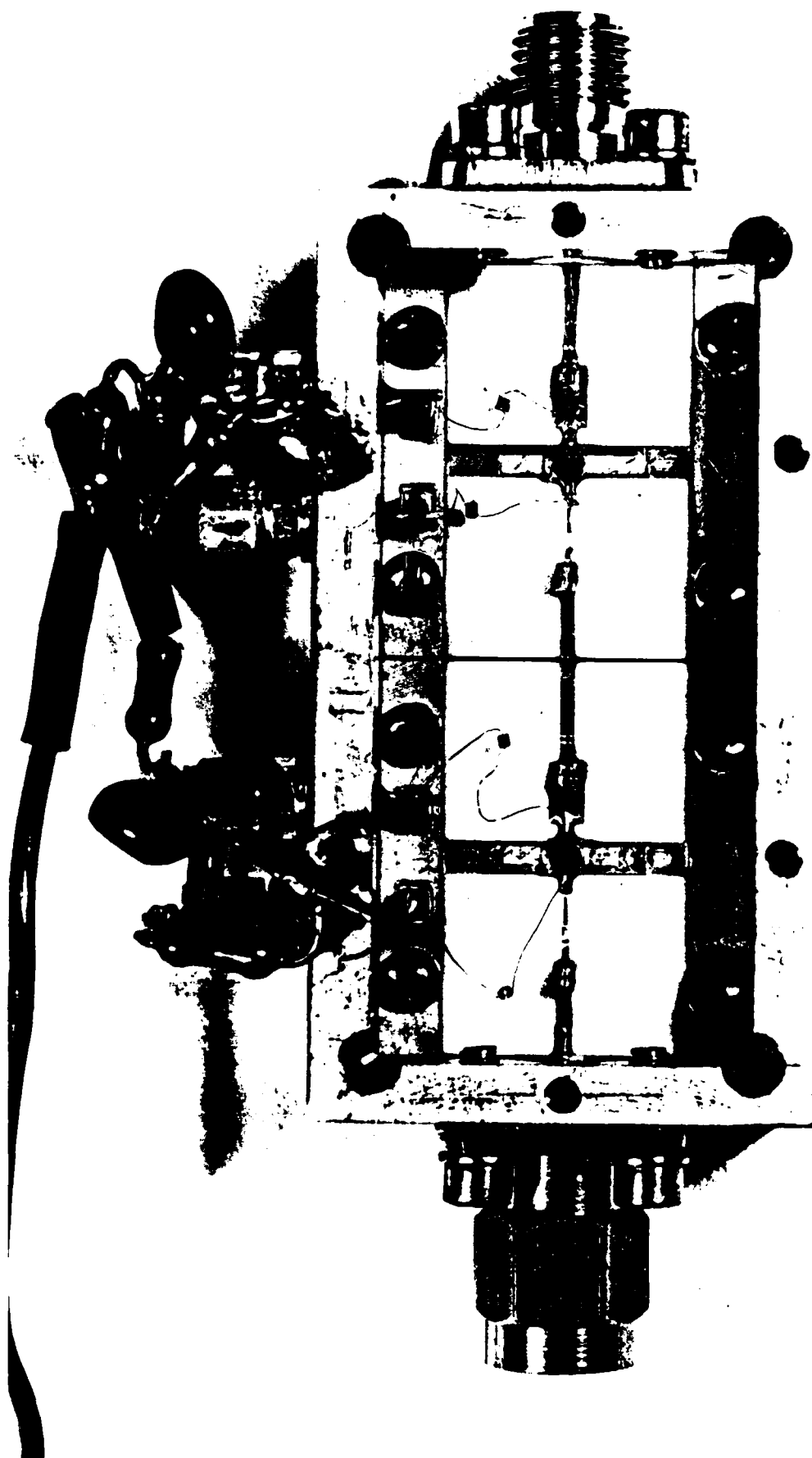
800 & 4000MHz
Antennas

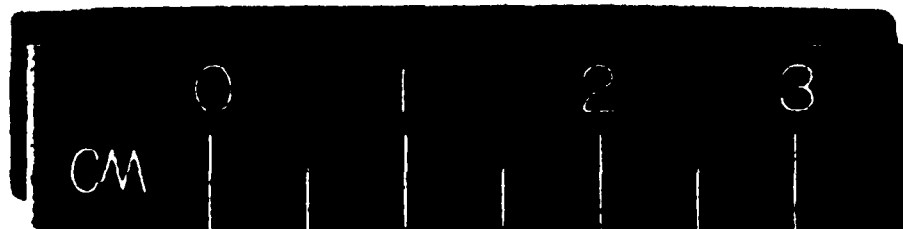
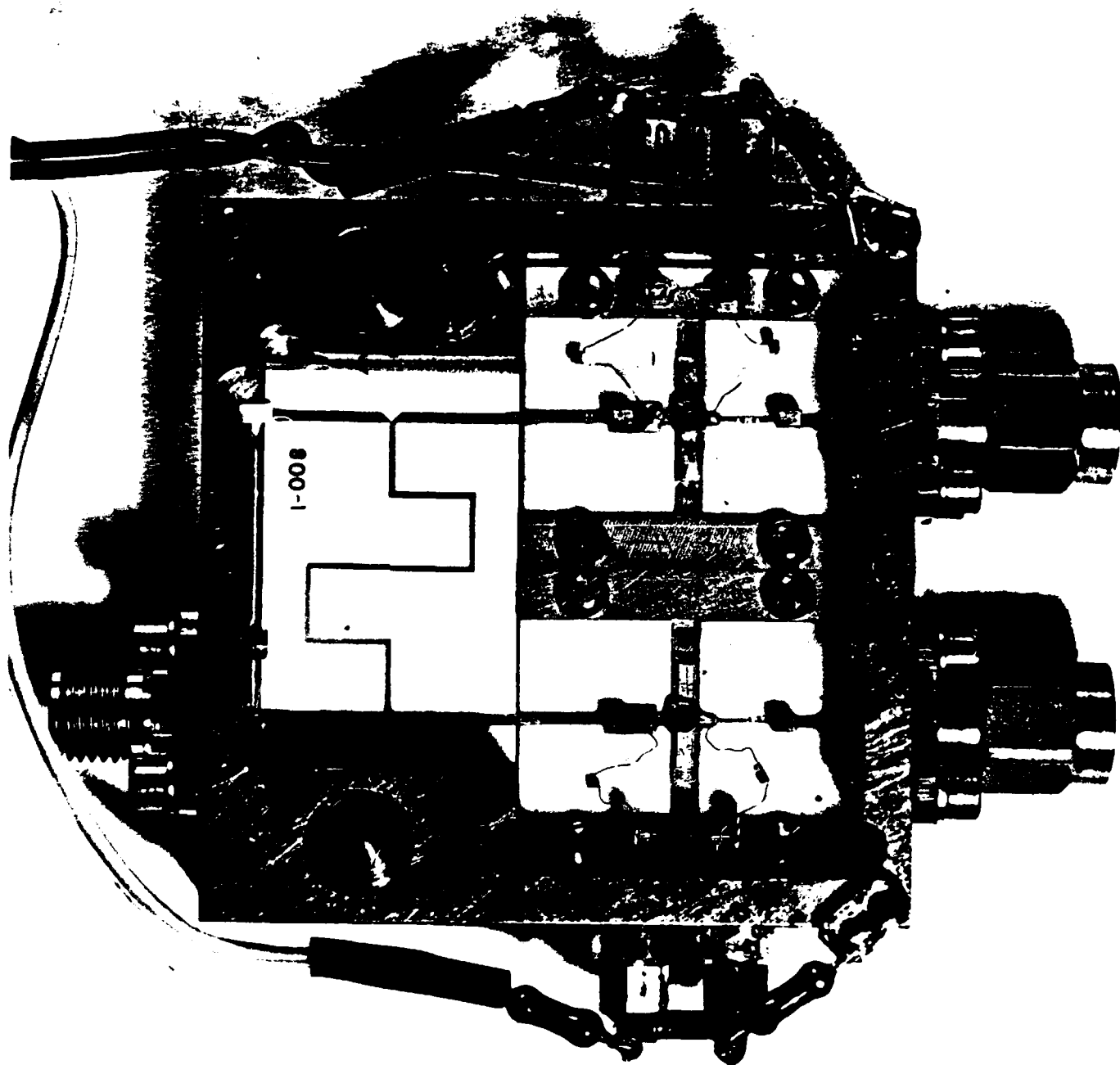


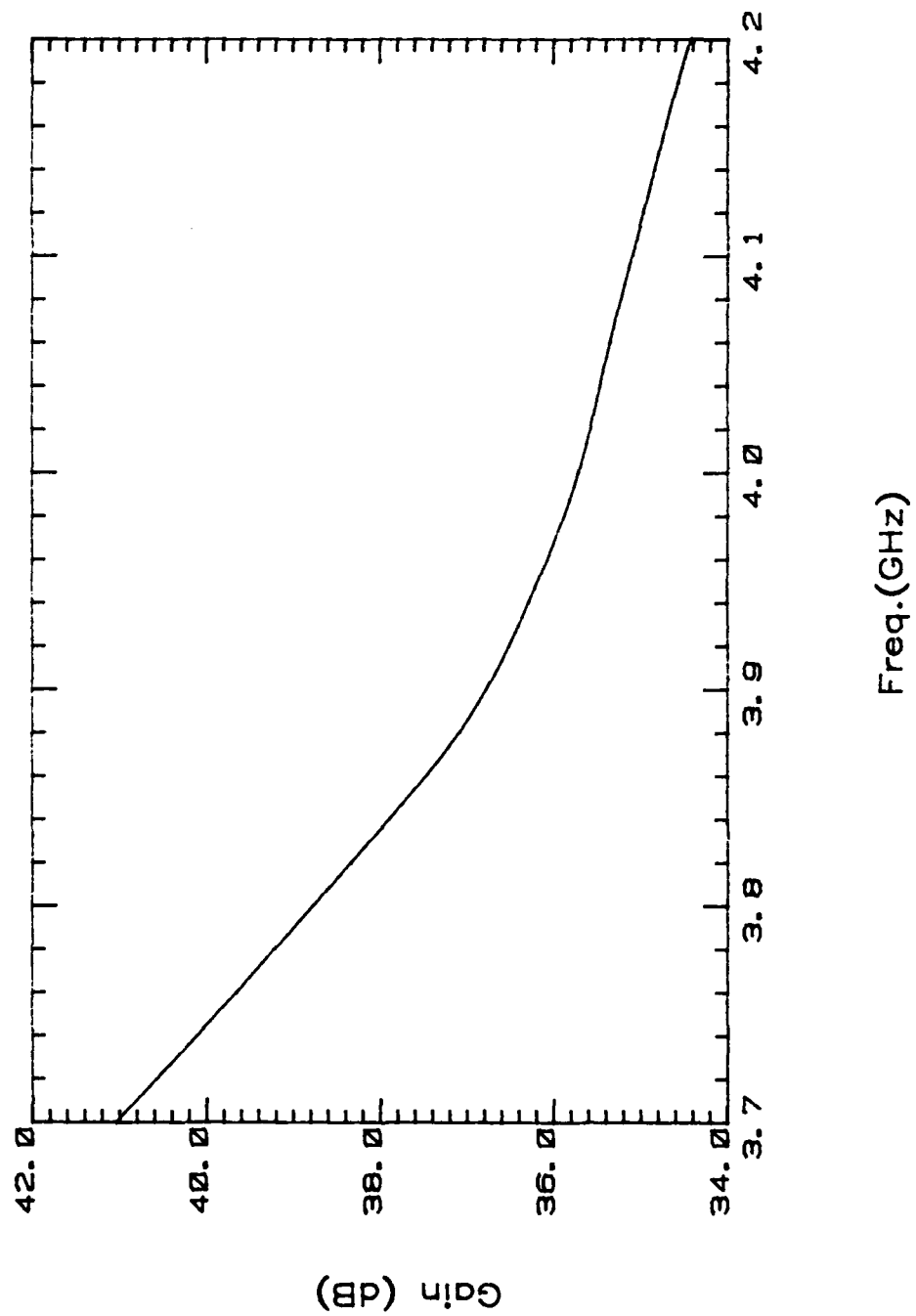


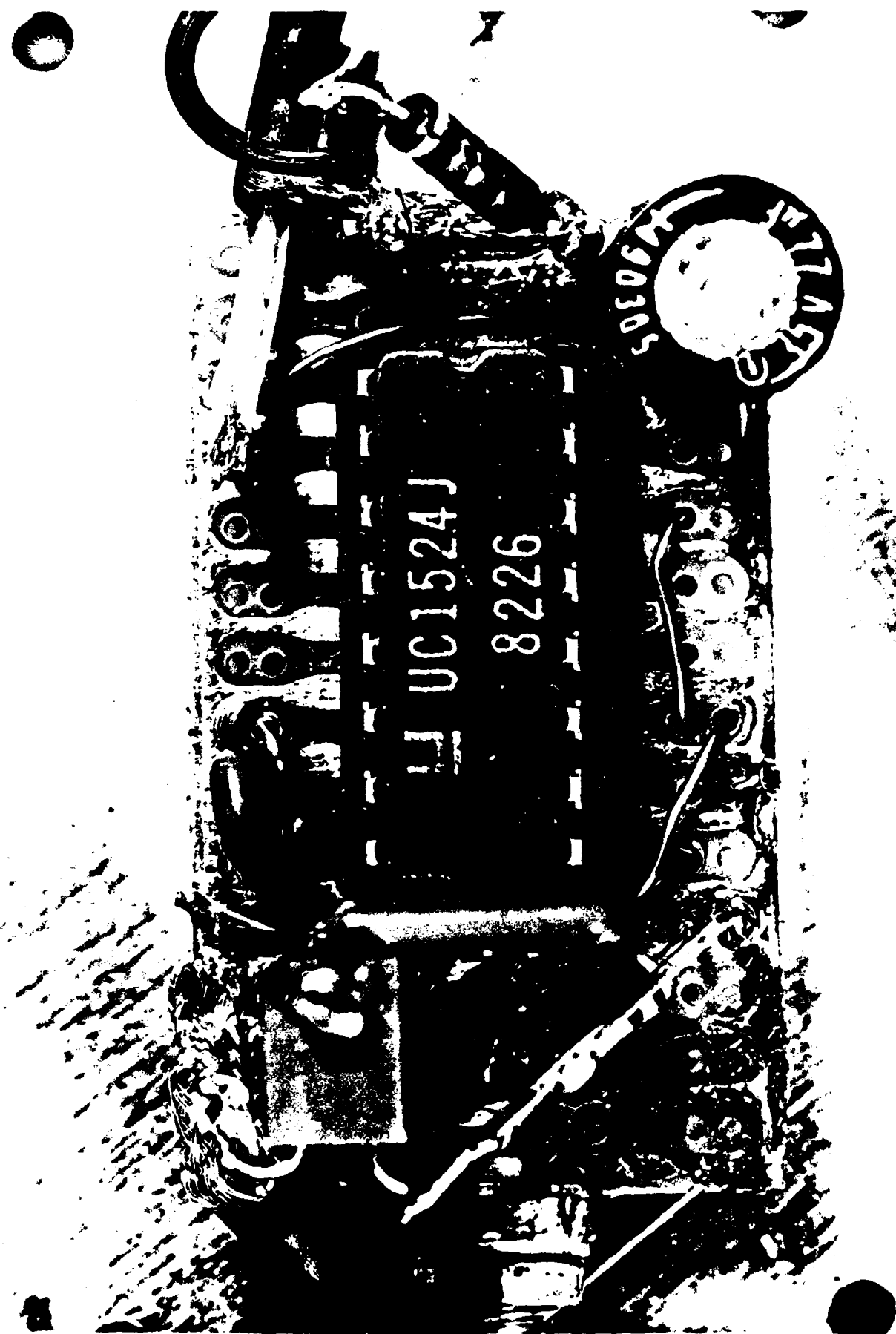


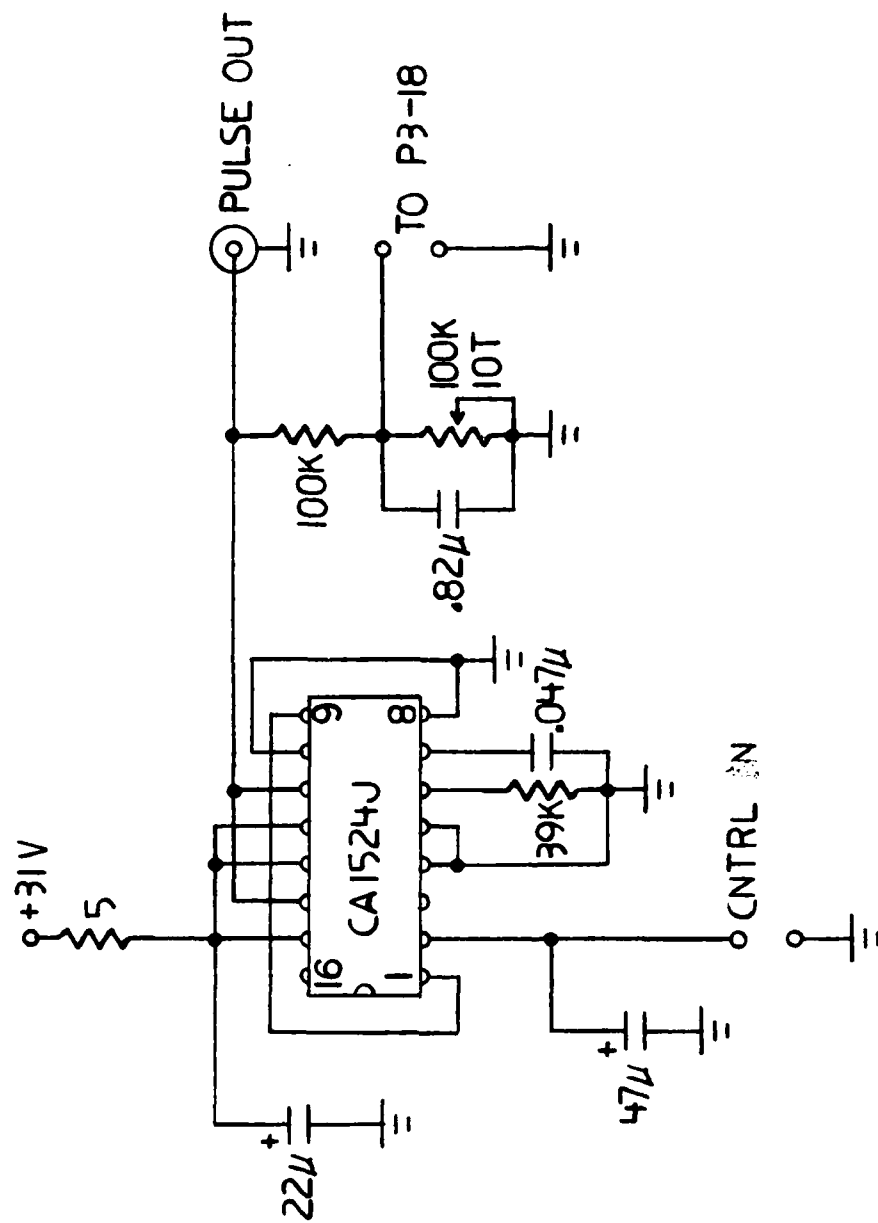


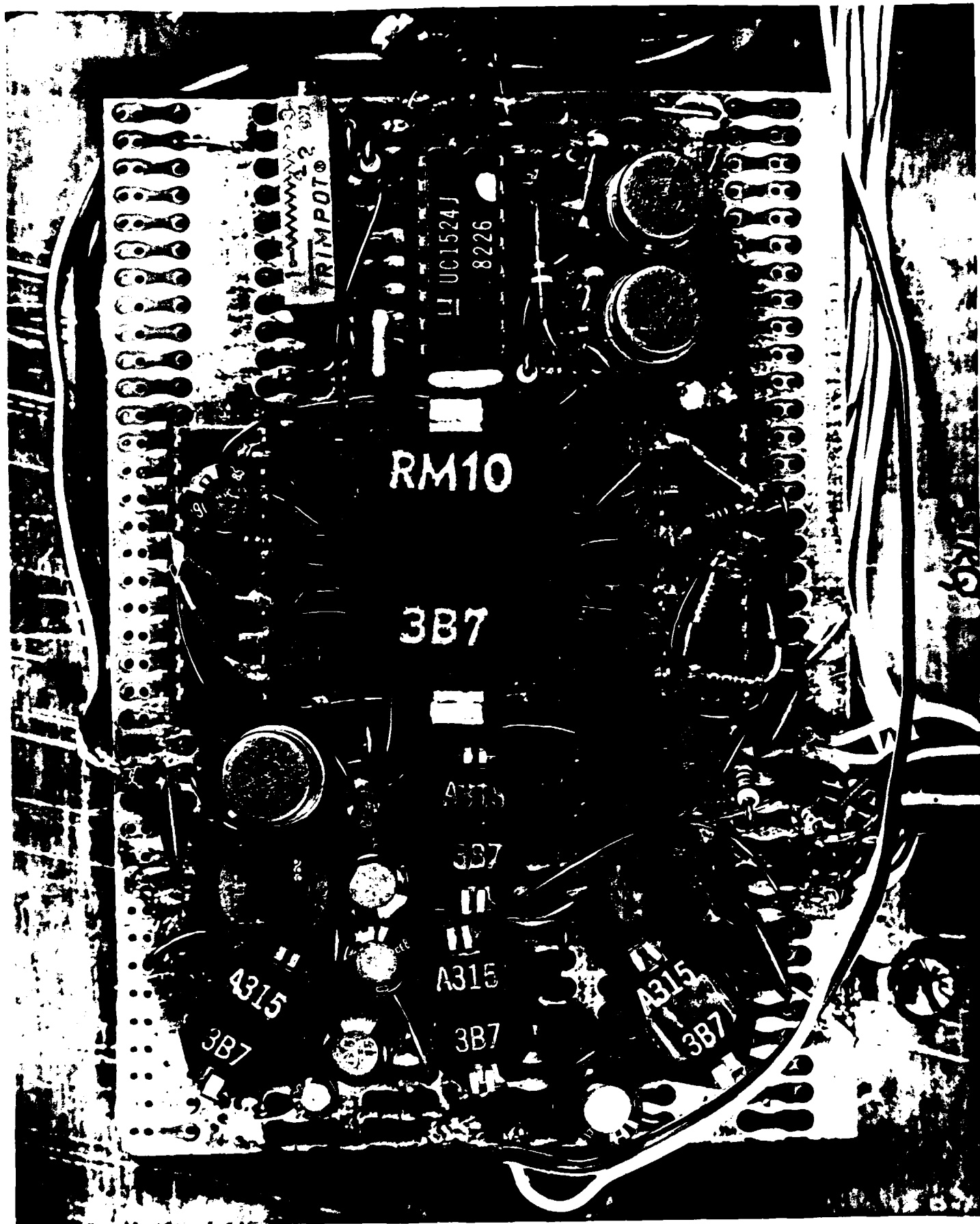












TRIMPO

UC1524J

8226

RM10

3B7

A315

3B7

A315

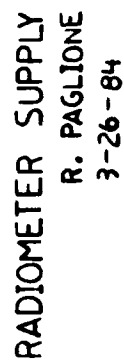
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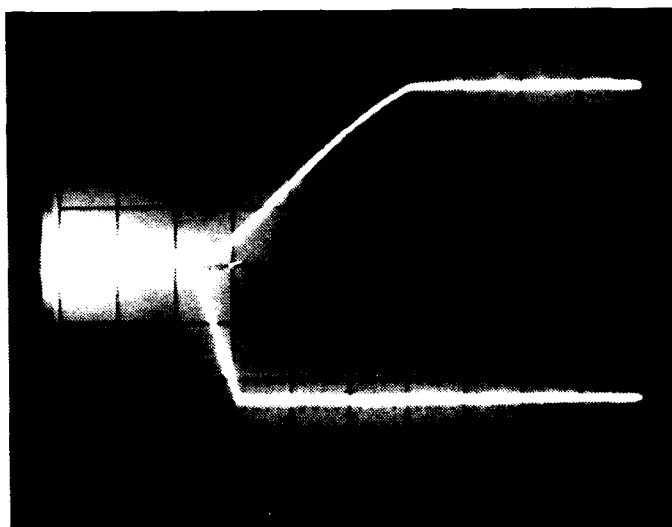
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3B7



" " 1964)HW85 = 47
(

(a)



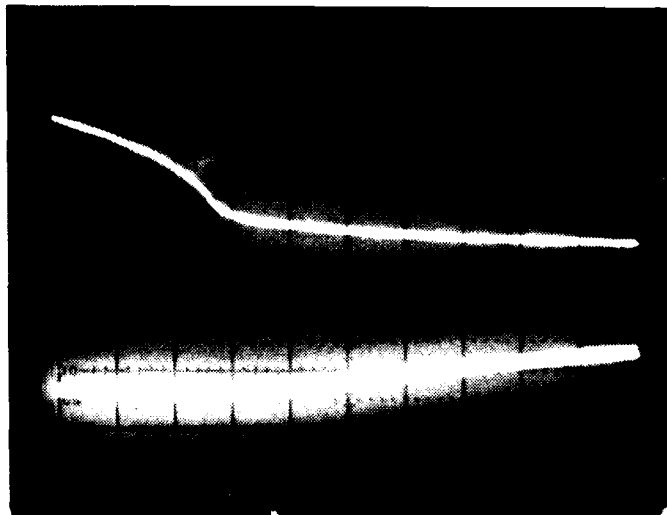
drain voltage
(1v/div)

turn-on

gate voltage
(2v/div)

time scale=20msec/div

(b)

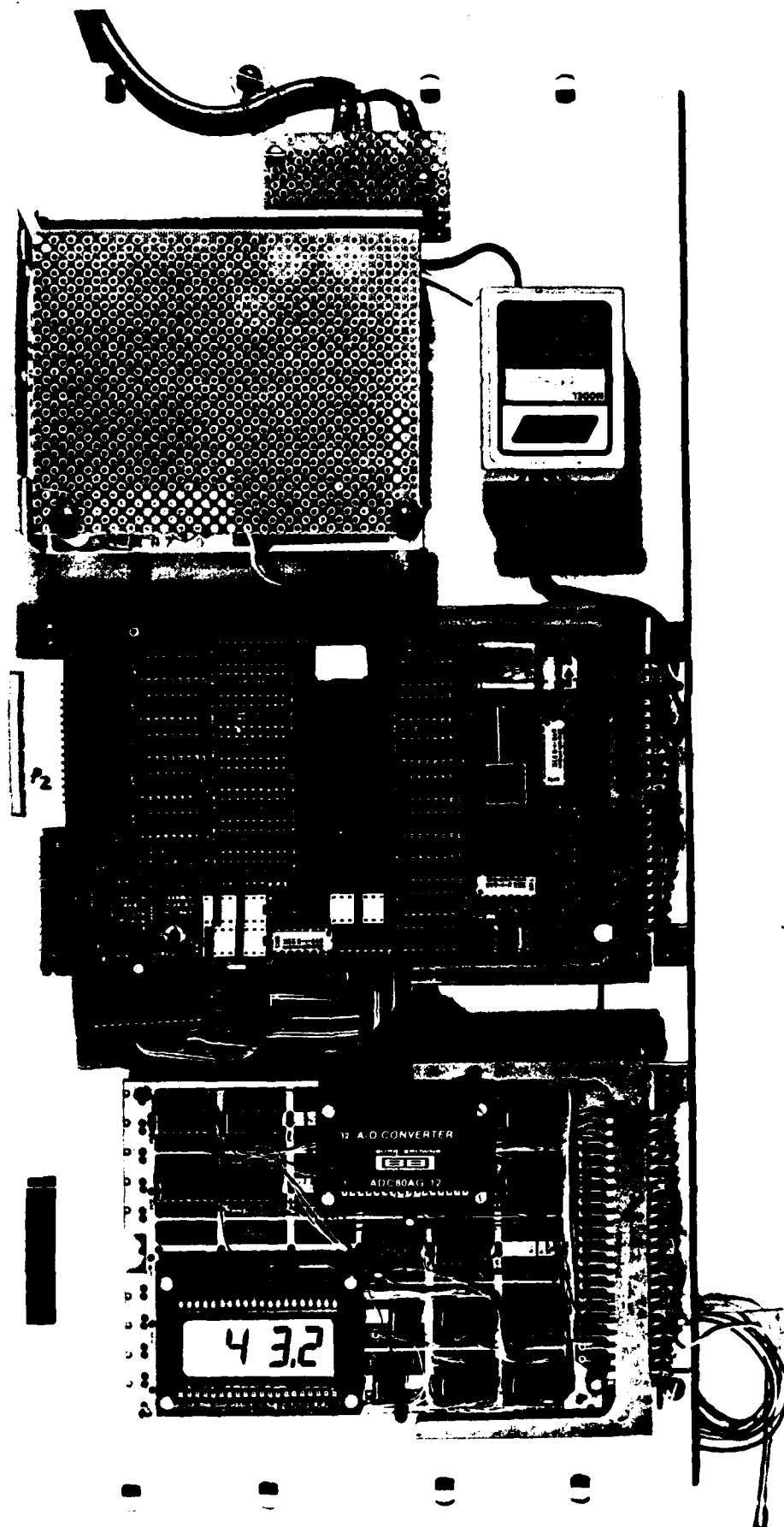


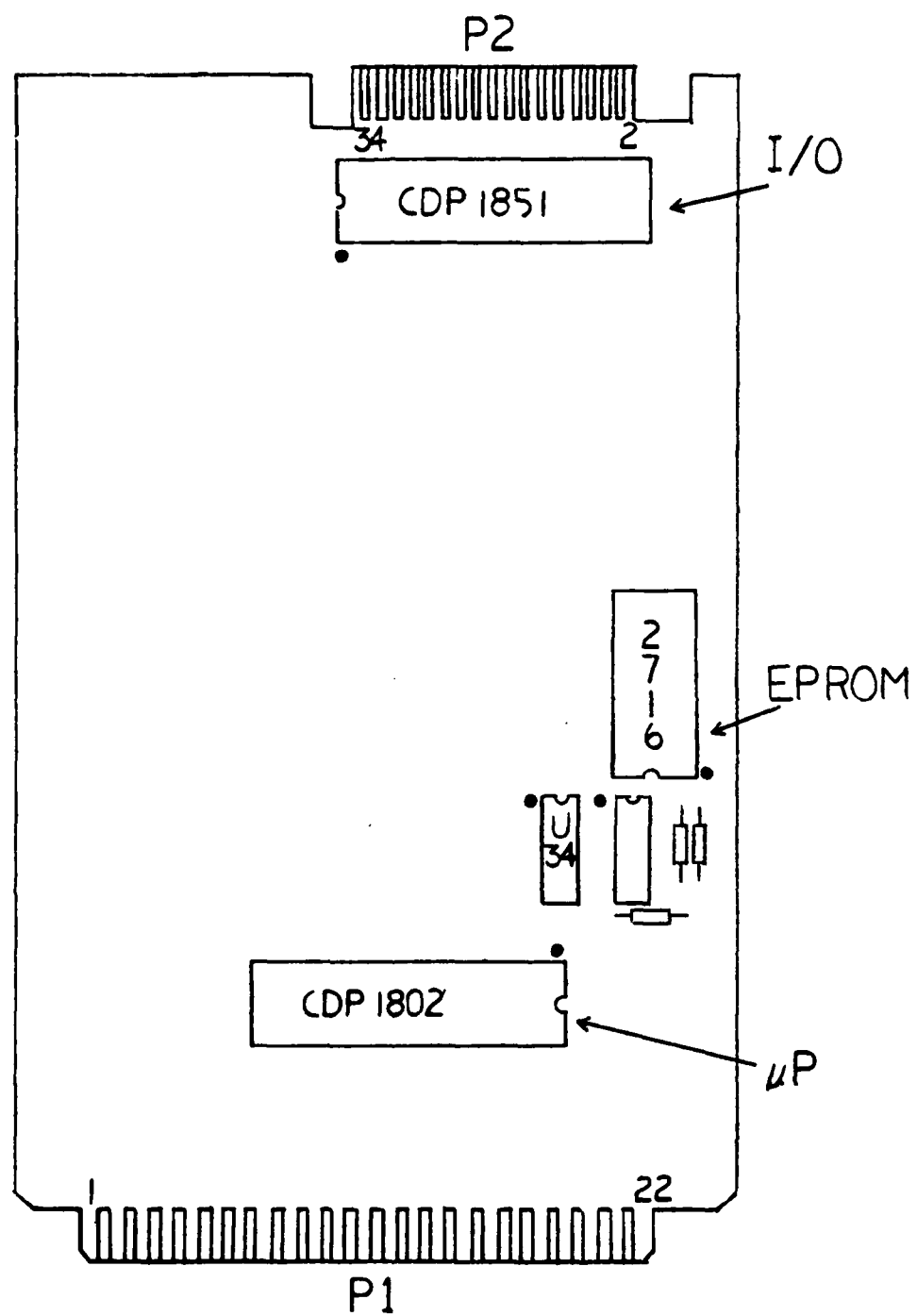
drain voltage
(1v/div)

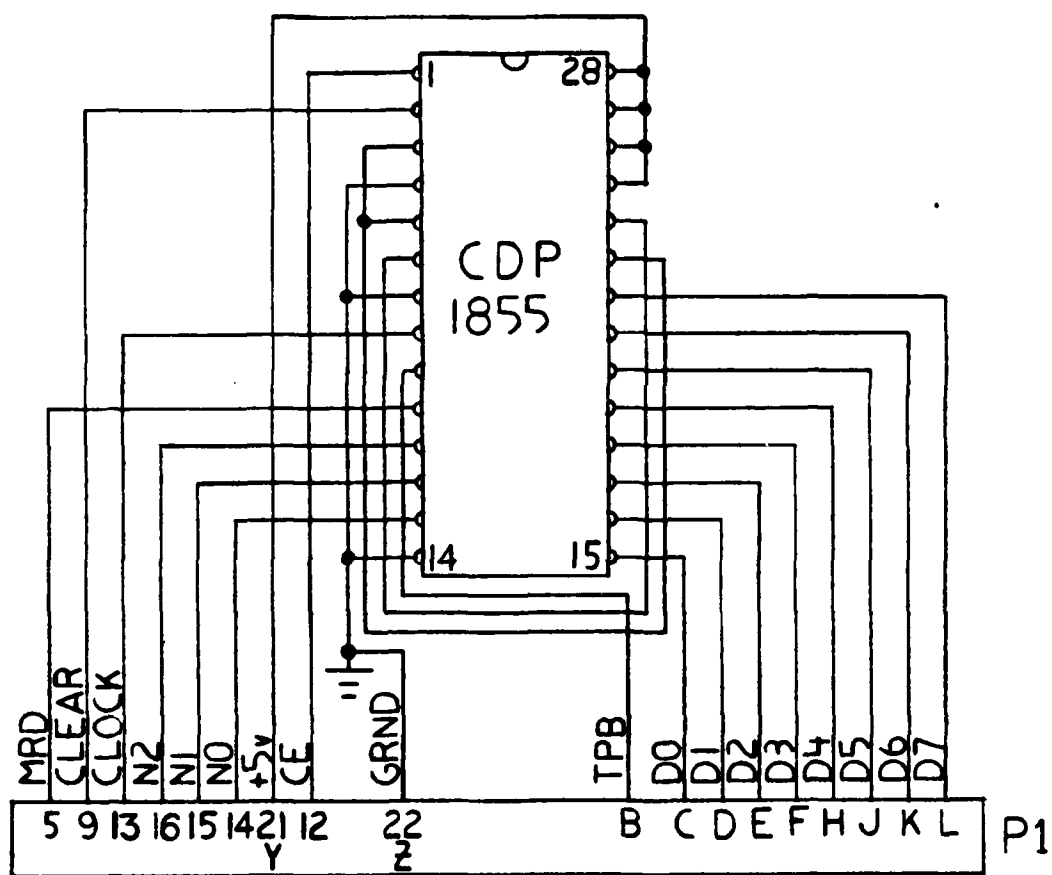
turn-off

gate voltage
(2v/div)

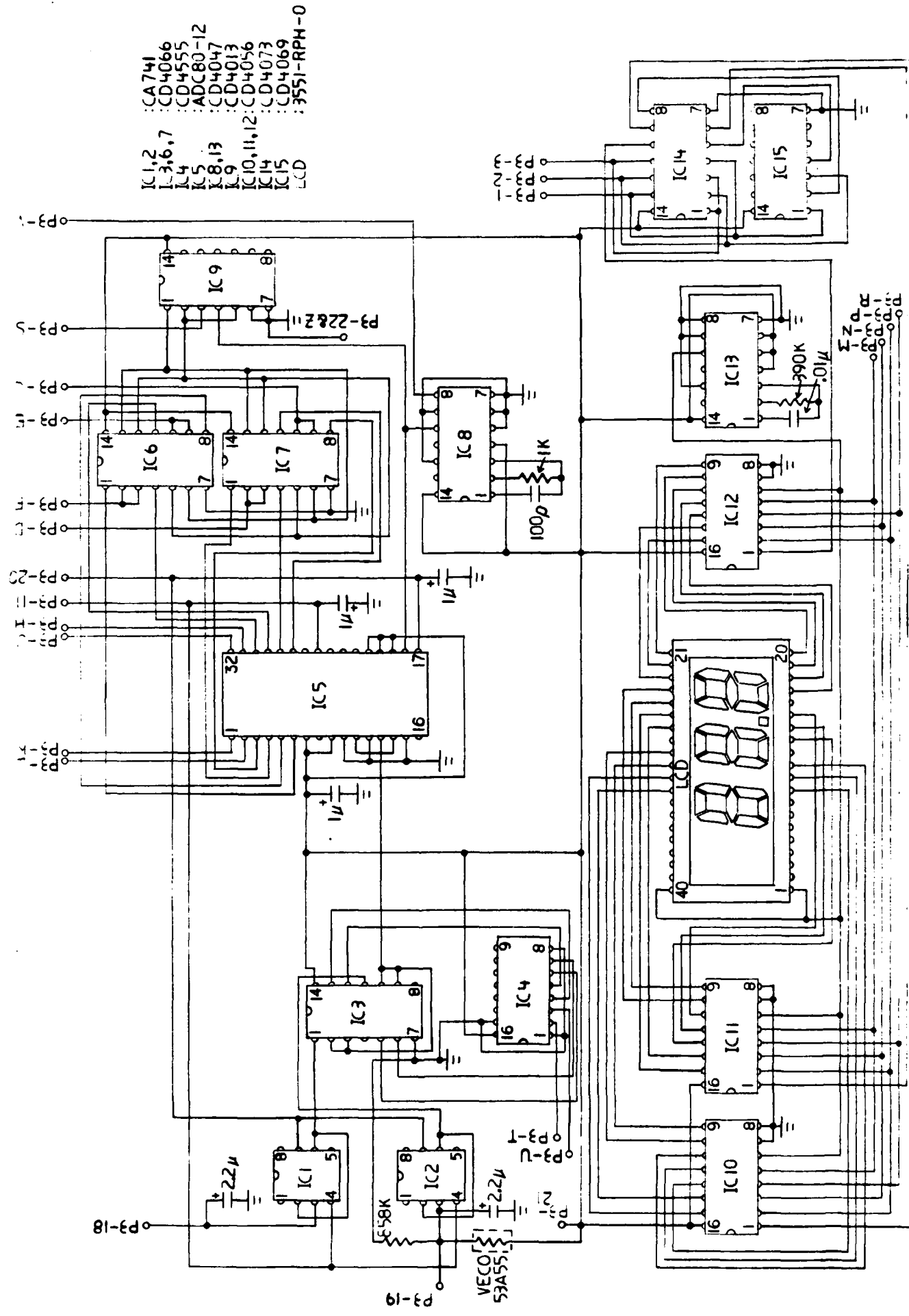
time scale=2msec/div

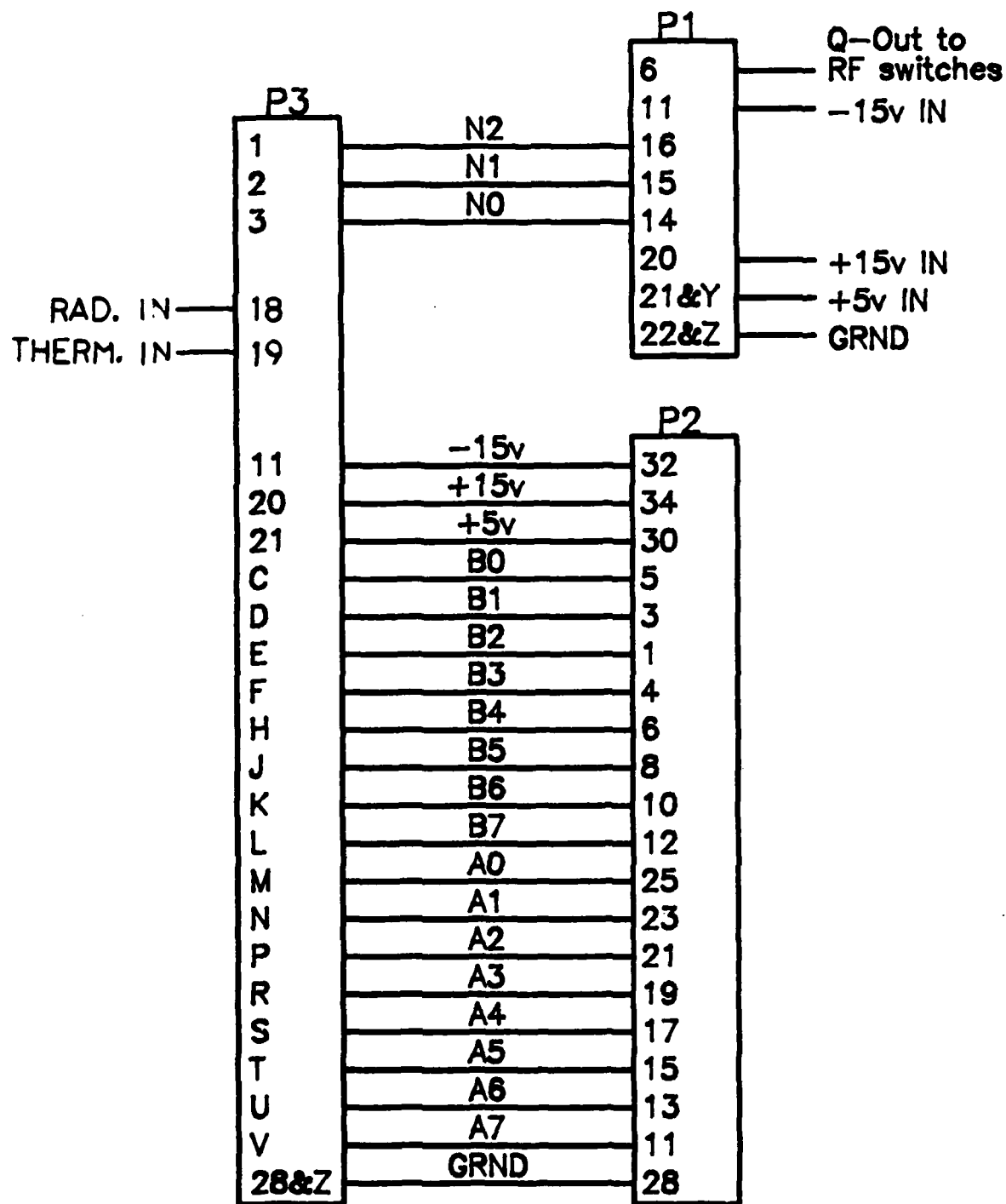


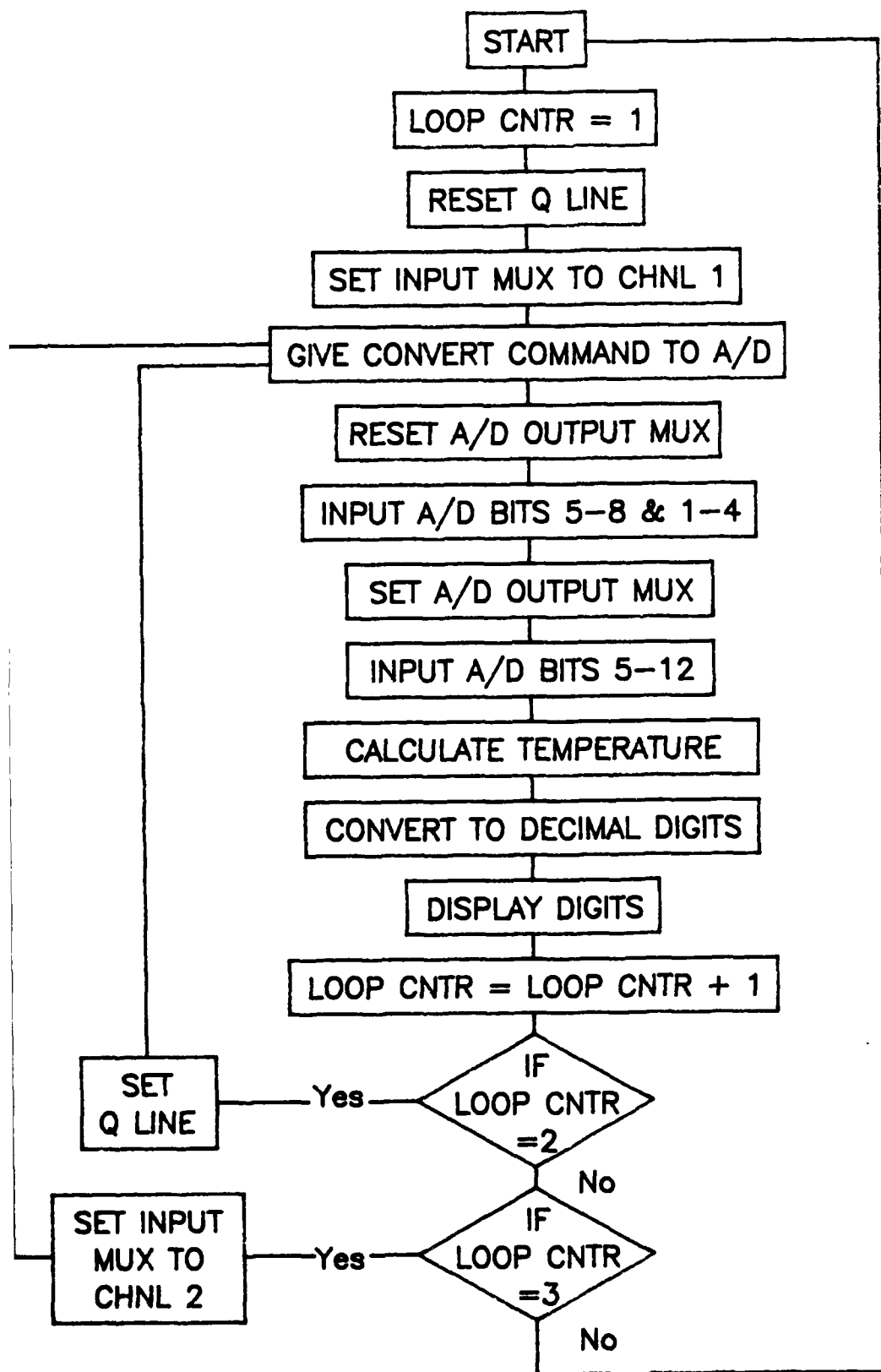


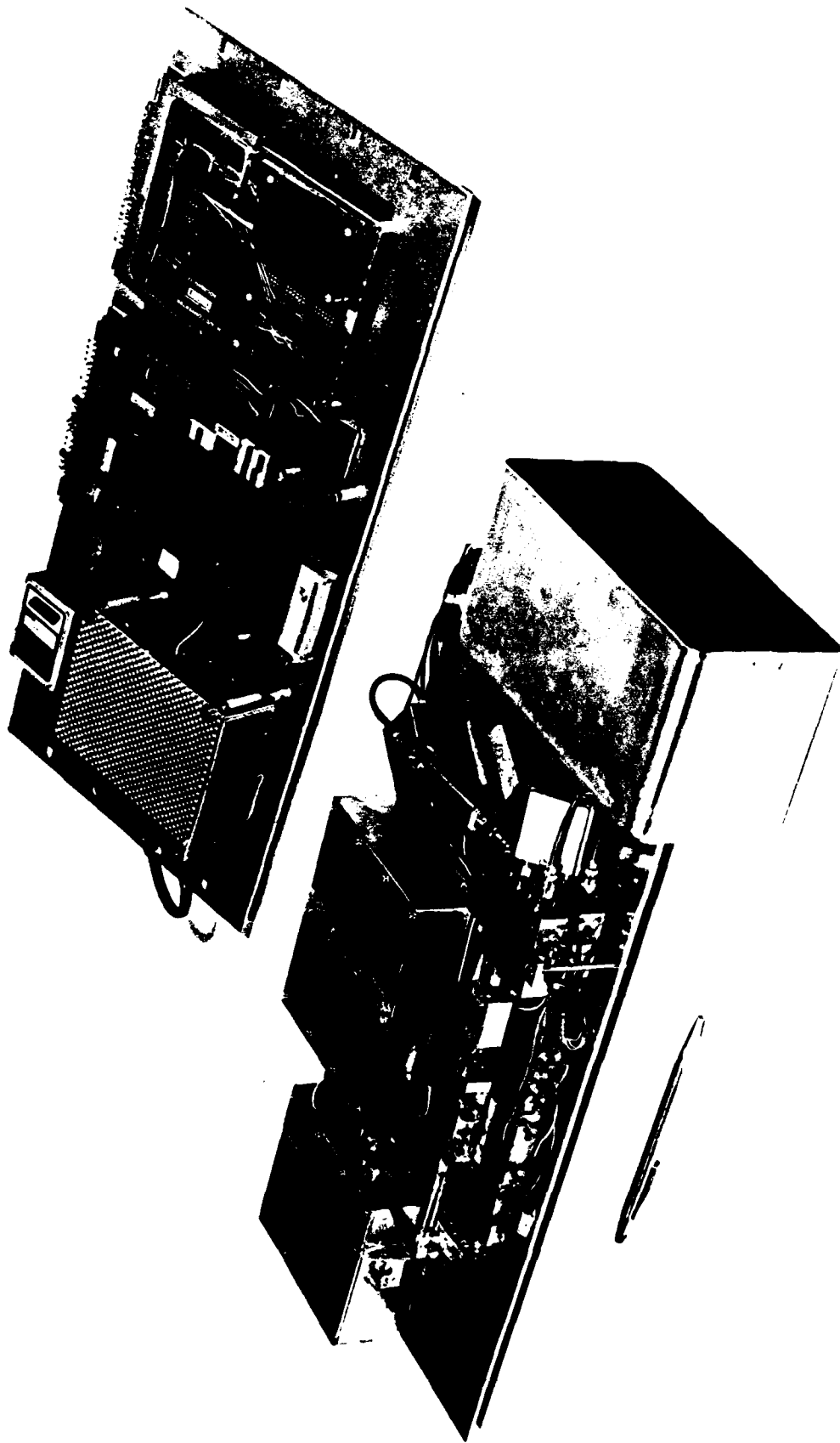


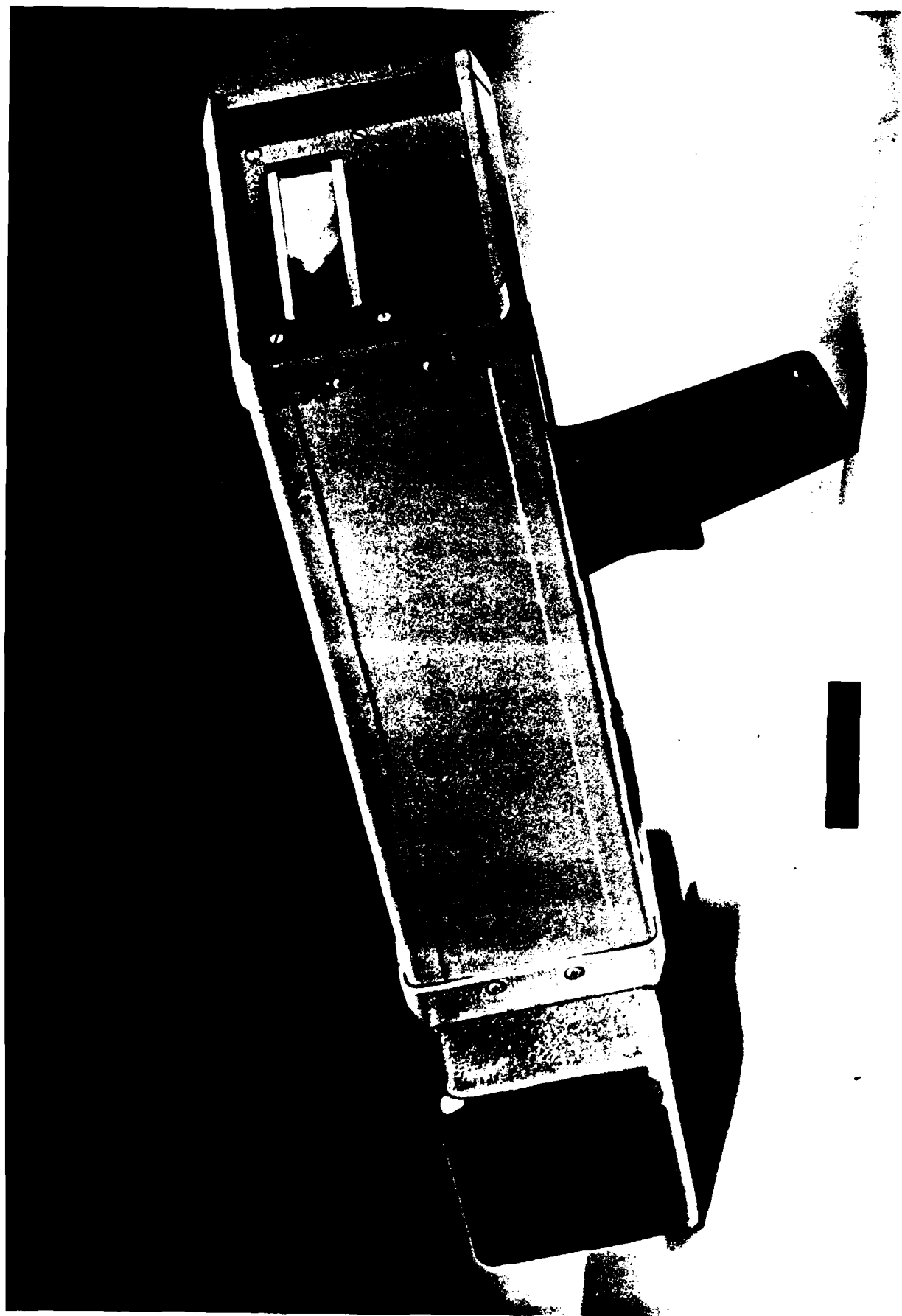
FROM U34
PIN 2
CDPI8S60I











- }. 30. a) Turn-on and b) turn-off characteristics of the +3v and -5v DC supplies in the switching regulator.
- }. 31. Photograph of the digital processor subsystem.
- }. 32. Layout of the major components on the CDP18S601 card.
- }. 33. Wiring diagram for the CDP1855 multiply/divide unit.
- }. 34. Schematic diagram for the interface and display card.
- }. 35. Interconnection diagram for the card-edge connectors in the digital processor subsystem.
- }. 36. Flow chart for the operation of the software in the digital processor subsystem.
- }. 37. Photograph of the breadboard radiometer system.
- }. 38. Photograph of prototype unit.

END

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9-85

DTIC